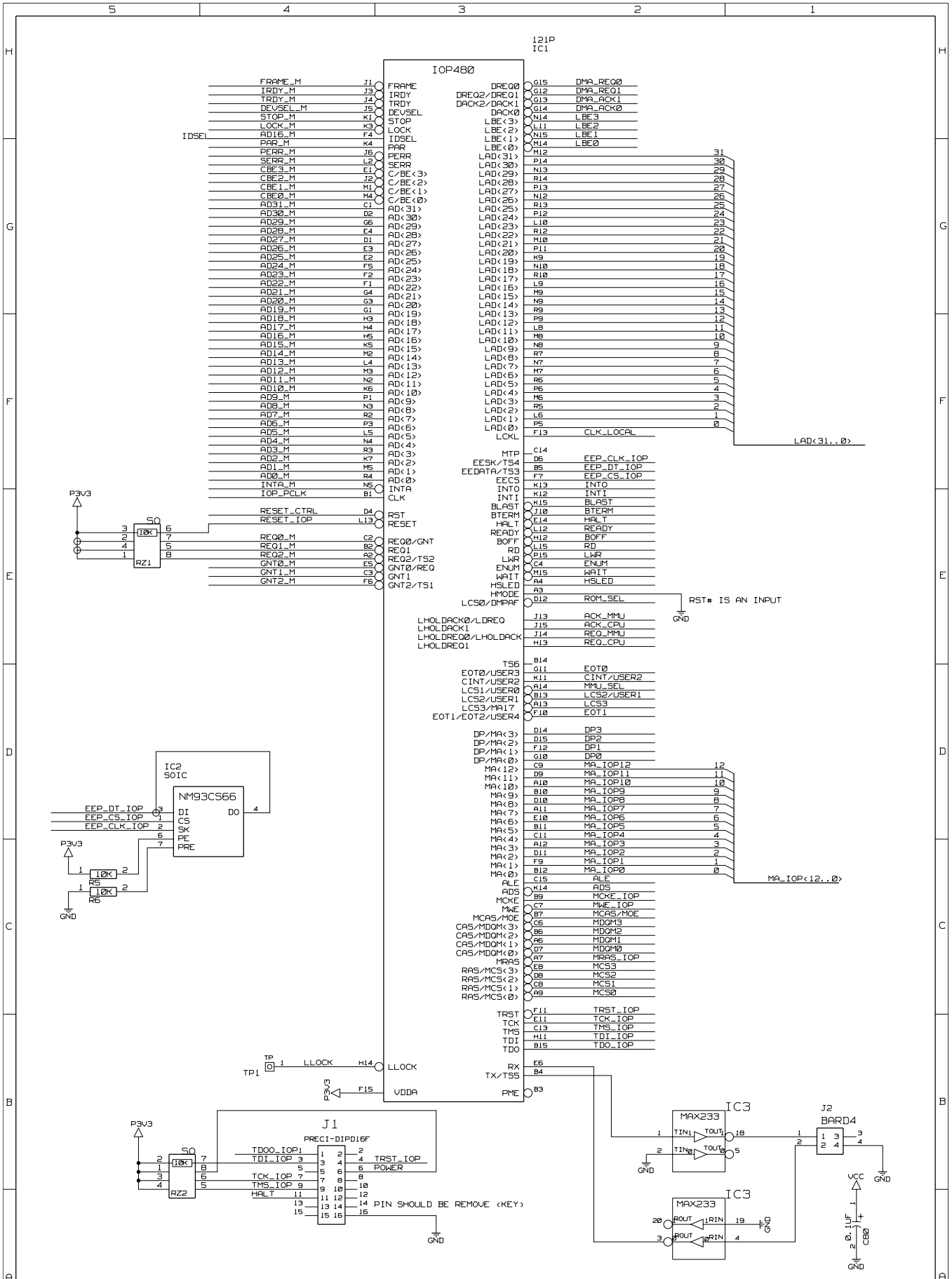
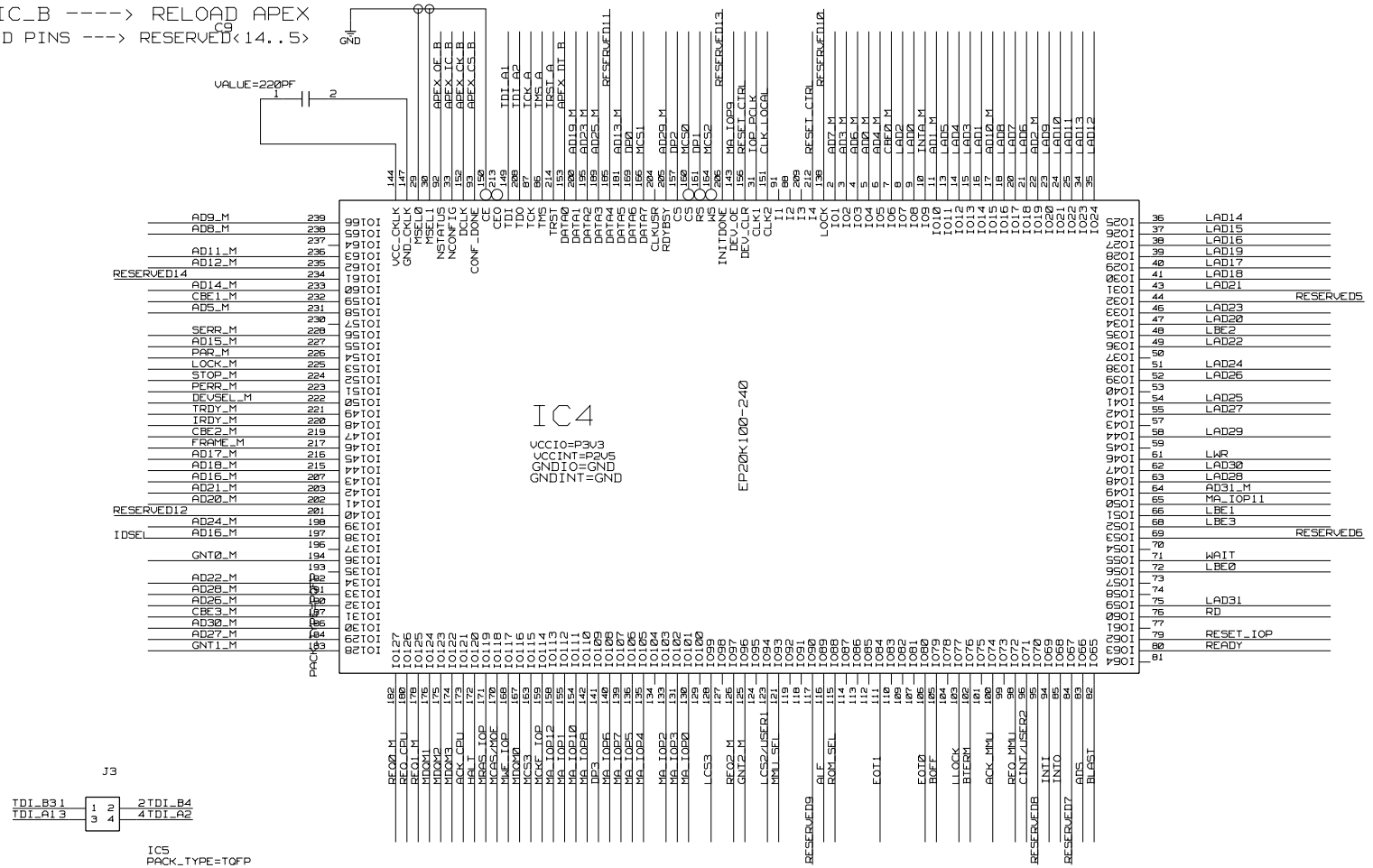

121P
IC1
IOP480
FRAME_M
IRDY_M
TRDY_M
DEVSEL_M
STOP_M
LOCK_M
AD16_M
PAR_M
PERR_M
SERR_M
CBE3_M
CBE2_M
CBE1_M
CBE0_M
AD31_M
AD30_M
AD29_M
AD28_M
AD27_M
AD26_M
AD25_M
AD24_M
AD23_M
AD22_M
AD21_M
AD20_M
AD19_M
AD18_M
AD17_M
AD16_M
AD15_M
AD14_M
AD13_M
AD12_M
AD11_M
AD10_M
AD9_M
AD8_M
AD7_M
AD6_M
AD5_M
AD4_M
AD3_M
AD2_M
AD1_M
AD0_M
INTA_M
IOP_PCLK
RESET_CTRL
RESET_IOP
REQ0_M
REQ1_M
REQ2_M
GNT0_M
GNT1_M
GNT2_M
IDSEL
FRAME
IRDY
TRDY
DEVSEL
STOP
LOCK
IDSEL
PAR
PERR
SERR
C/BE<3>
C/BE<2>
C/BE<1>
C/BE<0>
AD<31>
AD<30>
AD<29>
AD<28>
AD<27>
AD<26>
AD<25>
AD<24>
AD<23>
AD<22>
AD<21>
AD<20>
AD<19>
AD<18>
AD<17>
AD<16>
AD<15>
AD<14>
AD<13>
AD<12>
AD<11>
AD<10>
AD<9>
AD<8>
AD<7>
AD<6>
AD<5>
AD<4>
AD<3>
AD<2>
AD<1>
AD<0>
INTA
CLK
RST
RESET
REQ0/GNT
REQ1
REQ2/TS2
GNT0/REQ
GNT1
GNT2/TS1
DREQ0
DREQ2/DREQ1
DACK2/DACK1
DACK0
LBE<3>
LBE<2>
LBE<1>
LBE<0>
LAD<31>
LAD<30>
LAD<29>
LAD<28>
LAD<27>
LAD<26>
LAD<25>
LAD<24>
LAD<23>
LAD<22>
LAD<21>
LAD<20>
LAD<19>
LAD<18>
LAD<17>
LAD<16>
LAD<15>
LAD<14>
LAD<13>
LAD<12>
LAD<11>
LAD<10>
LAD<9>
LAD<8>
LAD<7>
LAD<6>
LAD<5>
LAD<4>
LAD<3>
LAD<2>
LAD<1>
LAD<0>
LCKL
MTP
EESK/TS4
EEDATA/TS3
EECS
INTO
INTI
BLAST
BTERM
HALT
READY
BOFF
RD
LWR
ENUM
WAIT
HSLED
HMODE
LCS0/DMPAF
LHOLDACK0/LDREQ
LHOLDACK1
LHOLDREQ0/LHOLDACK
LHOLDREQ1
TS6
EOT0/USER3
CINT/USER2
LCS1/USER0
LCS2/USER1
LCS3/MA17
EOT1/EOT2/USER4
DP/MA<3>
DP/MA<2>
DP/MA<1>
DP/MA<0>
MA<12>
MA<11>
MA<10>
MA<9>
MA<8>
MA<7>
MA<6>
MA<5>
MA<4>
MA<3>
MA<2>
MA<1>
MA<0>
ALE
ADS
MCKE
MWE
MCAS/MOE
CAS/MDQM<3>
CAS/MDQM<2>
CAS/MDQM<1>
CAS/MDQM<0>
MRAS
RAS/MCS<3>
RAS/MCS<2>
RAS/MCS<1>
RAS/MCS<0>
TRST
TCK
TMS
TDI
TDO
RX
TX/TS5
PME
LLOCK
VDDA
CLK_LOCAL
EEP_CLK_IOP
EEP_DT_IOP
EEP_CS_IOP
INTO
INTI
BLAST
BTERM
HALT
READY
BOFF
RD
LWR
ENUM
WAIT
HSLED
ROM_SEL
RST# IS AN INPUT
ACK_MMU
ACK_CPU
REQ_MMU
REQ_CPU
EOT0
CINT/USER2
MMU_SEL
LCS2/USER1
LCS3
EOT1
DP3
DP2
DP1
DP0
MA_IOP12
MA_IOP11
MA_IOP10
MA_IOP9
MA_IOP8
MA_IOP7
MA_IOP6
MA_IOP5
MA_IOP4
MA_IOP3
MA_IOP2
MA_IOP1
MA_IOP0
ALE
ADS
MCKE_IOP
MWE_IOP
MCAS/MOE
MDQM3
MDQM2
MDQM1
MDQM0
MRAS_IOP
MCS3
MCS2
MCS1
MCS0
TRST_IOP
TCK_IOP
TMS_IOP
TDI_IOP
TDO_IOP
LAD<31..0>
MA_IOP<12..0>
P3V3
SO
10K
RZ1
IC2
SOIC
NM93CS66
DI
CS
SK
PE
PRE
DO
R5
R6
GND
TP1
TP
LLOCK
J1
PRECI-DIPD16F
TDO0_IOP
TDI_IOP
TRST_IOP
POWER
TCK_IOP
TMS_IOP
HALT
PIN SHOULD BE REMOVE (KEY)
RZ2
IC3
MAX233
TIN1
TIN2
TOUT1
TOUT2
J2
BARD4
VCC
0.1UF
CB0
REF:
DIV.
CN/CE
CERN
1211 GENEVA 23
SWITZERLAND
DRAWING TITLE:
RUM_01
ABBREV:
IOP480_PROCESSOR
PAGE:
1 OF 20
LAST_MODIFIED=Fri May 5 11:53:58 2000
DESSIN:
ETUDE:
DATE:

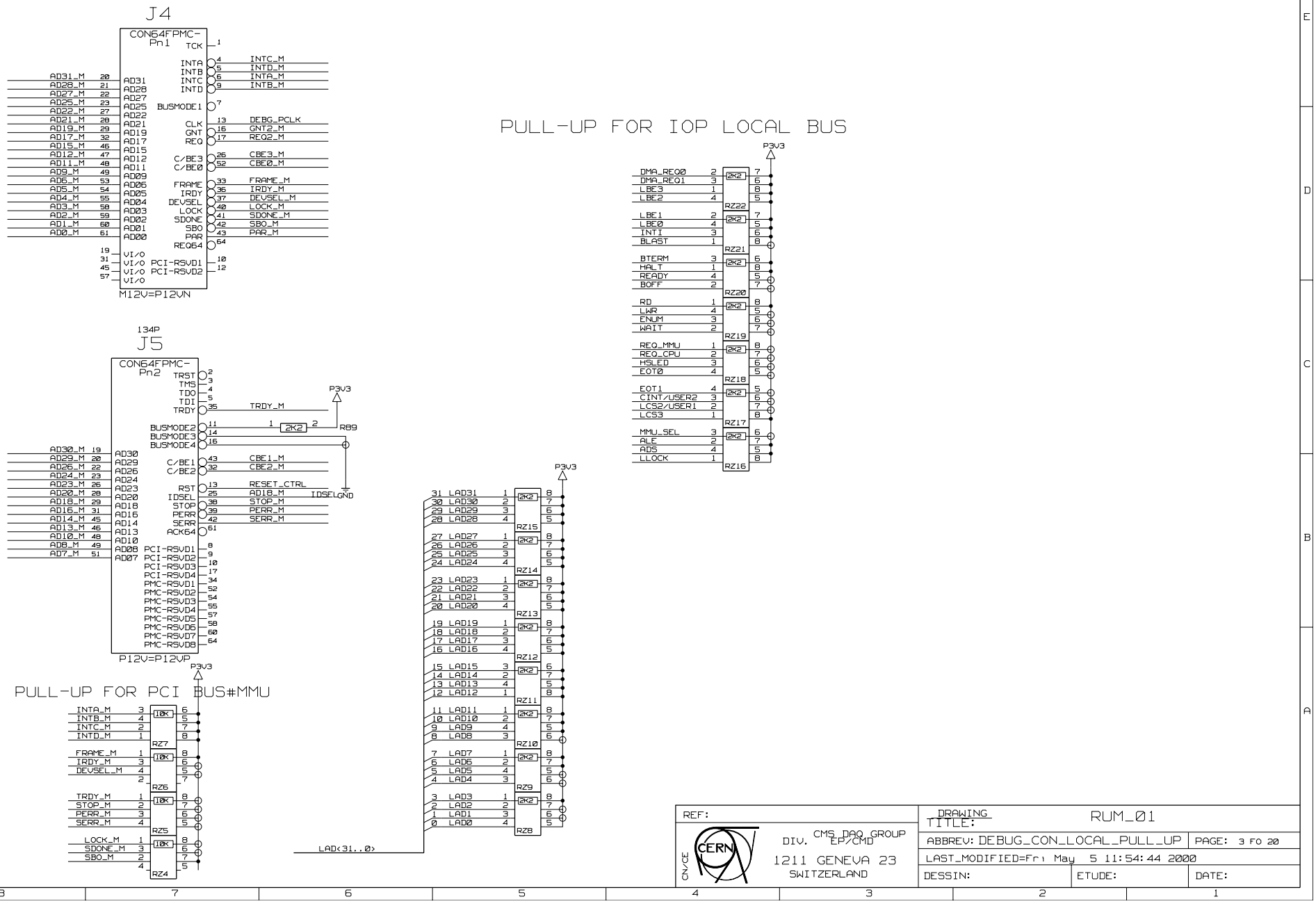
CHAIN A TDI_A1---->TDI_A2
CHAIN B TDI_B3---->TDI_B4

APEX_IC_B ----> RELOAD APEX
RESERVED PINS ---> RESERVED<14..5>



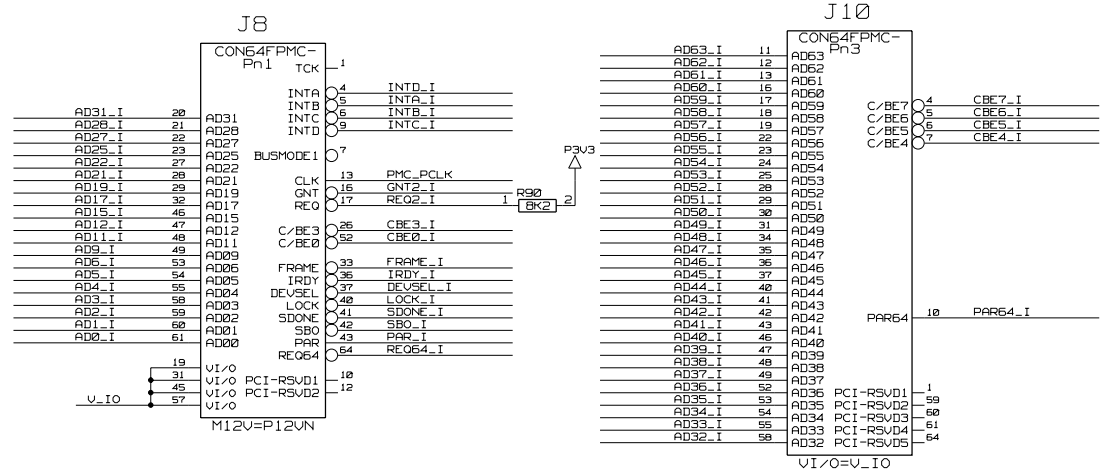
REF:	DRAWING TITLE:	RUM_01	
CERN DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: FPGA_IOP		PAGE: 2 OF 20
	LAST_MODIFIED=Fri May 5 11:54:26 2000		
	DESSIN:	ETUDE:	DATE:

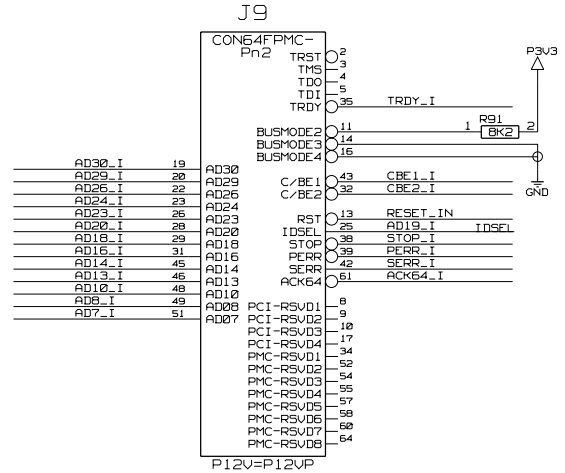
PCI BUS#MMU DEBUGGER CONNECTORS

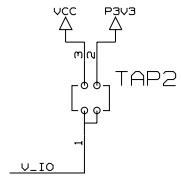


REF:	CERN CN/CE DIV. CMS DAQ GROUP EP/CMD 1211 GENEVA 23 SWITZERLAND	DRAWING TITLE:	RUM_01
		ABBREV: DEBUG_CON_LOCAL_PULL_UP	PAGE: 3 Fo 20
		LAST_MODIFIED=Fri May 5 11:54:44 2000	
		DESSIN:	ETUDE: DATE:

PMC CONNECTORS INPUT DATA BUS

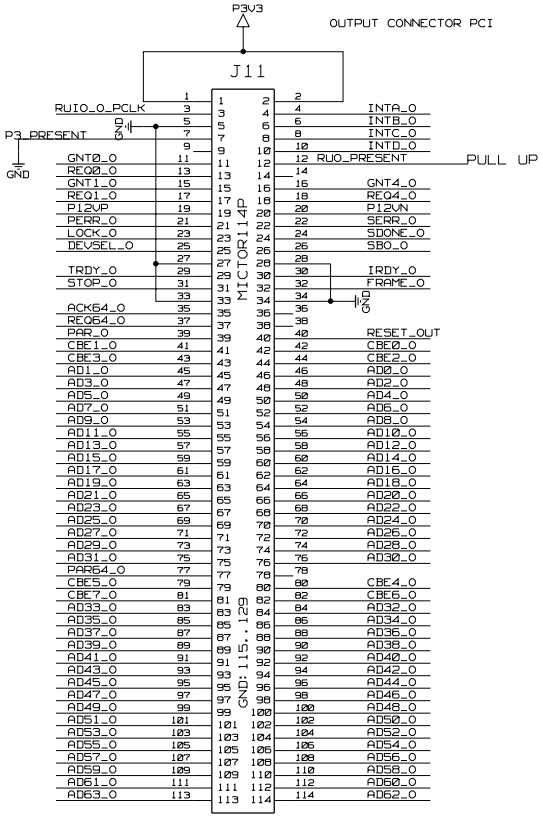


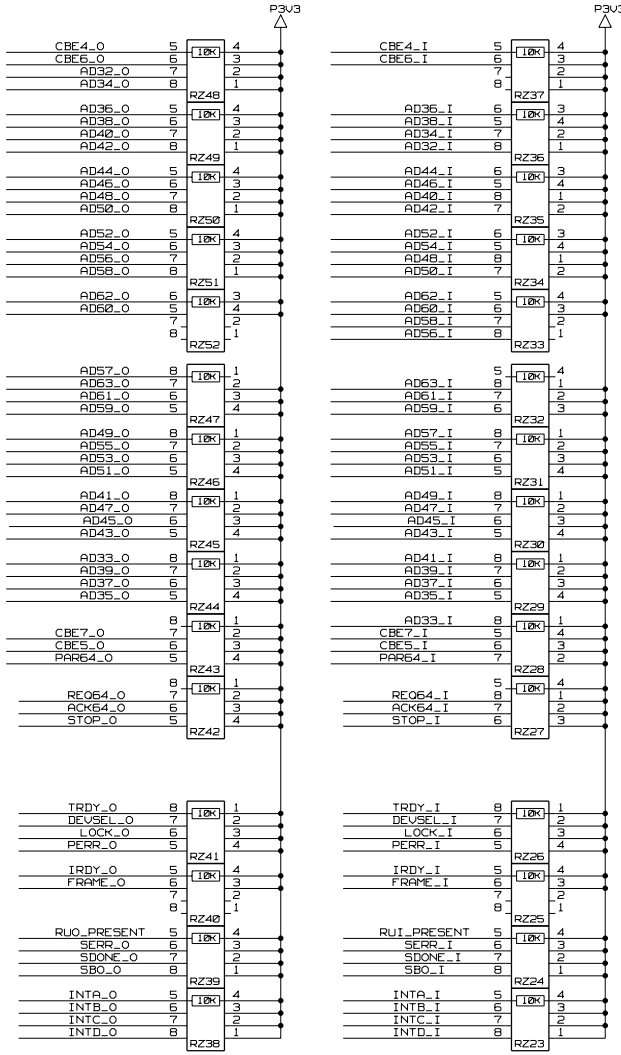




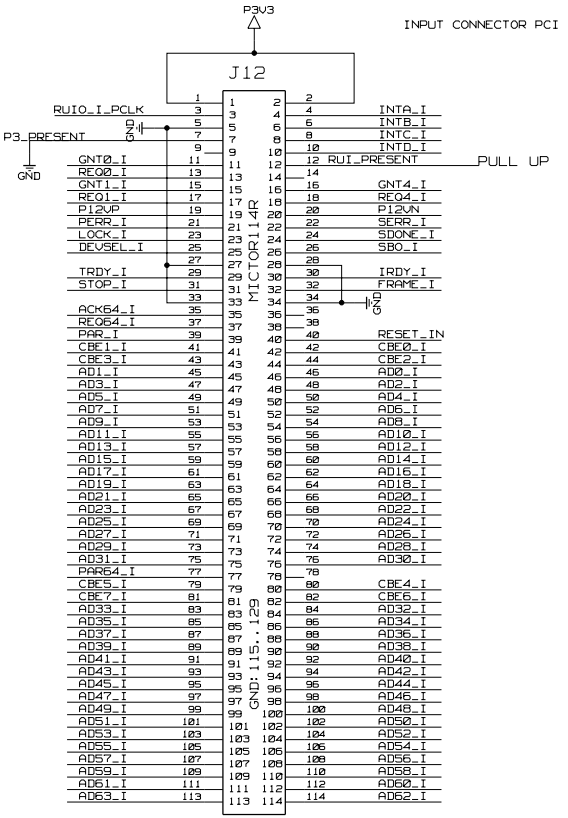
REF:	DRAWING TITLE: RUM_01	
CERN DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: SECOND_PCI_BUS_CONNECTORS	PAGE: 4 OF 20
	LAST_MODIFIED=Fri May 5 11:55:13 2000	
	DESSIN:	ETUDE: DATE:

CONNECTOR FOR RUO EXTENSION

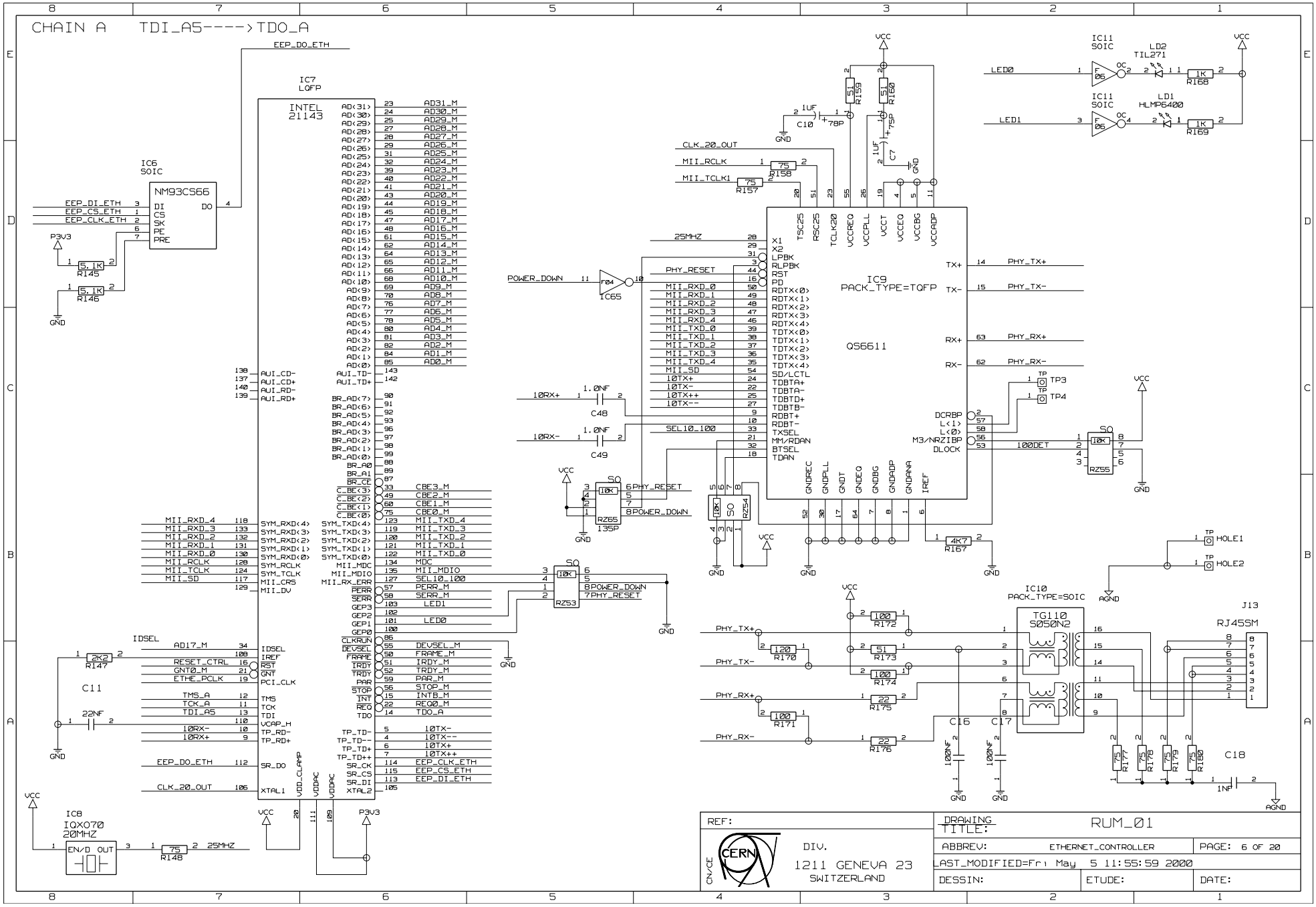


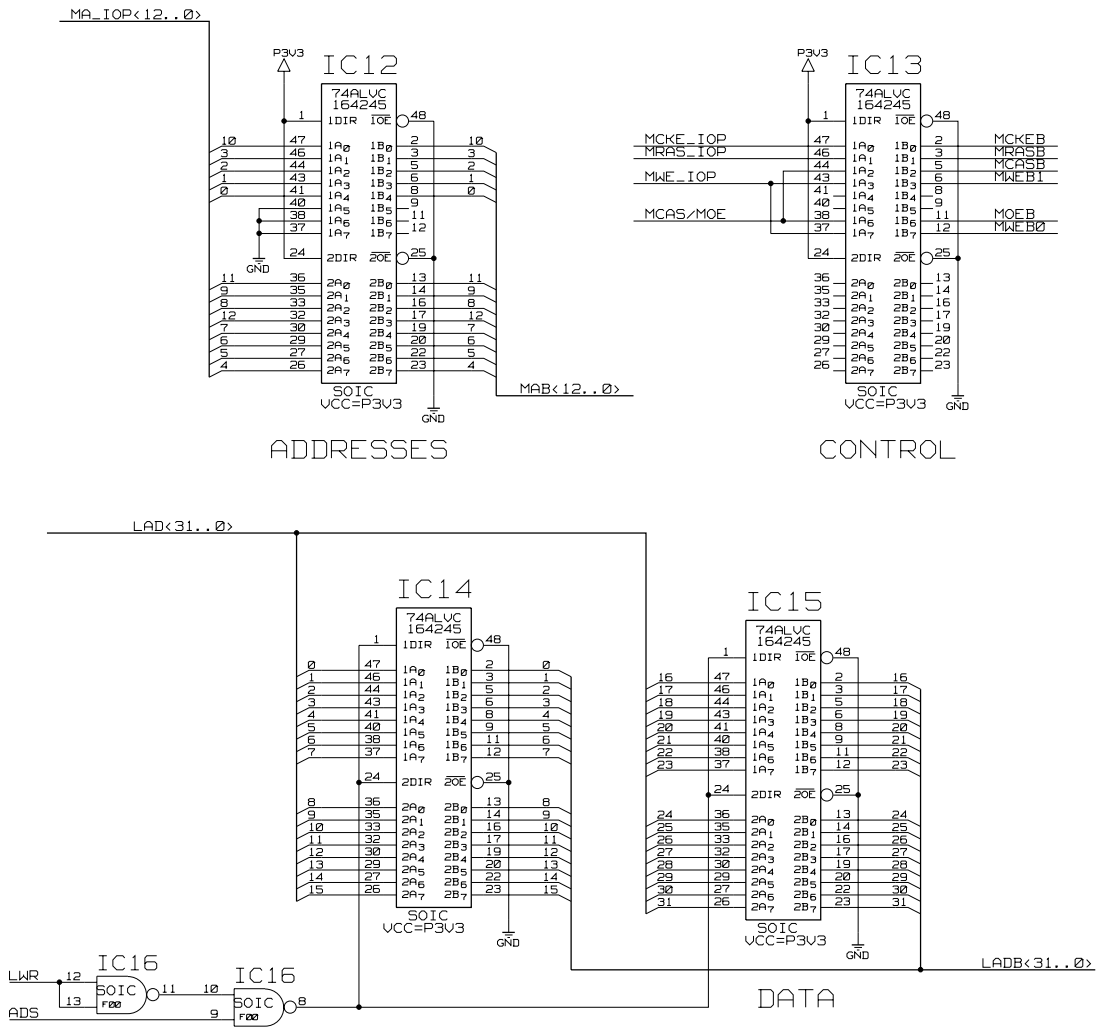


CONNECTOR FOR RUI EXTENSION



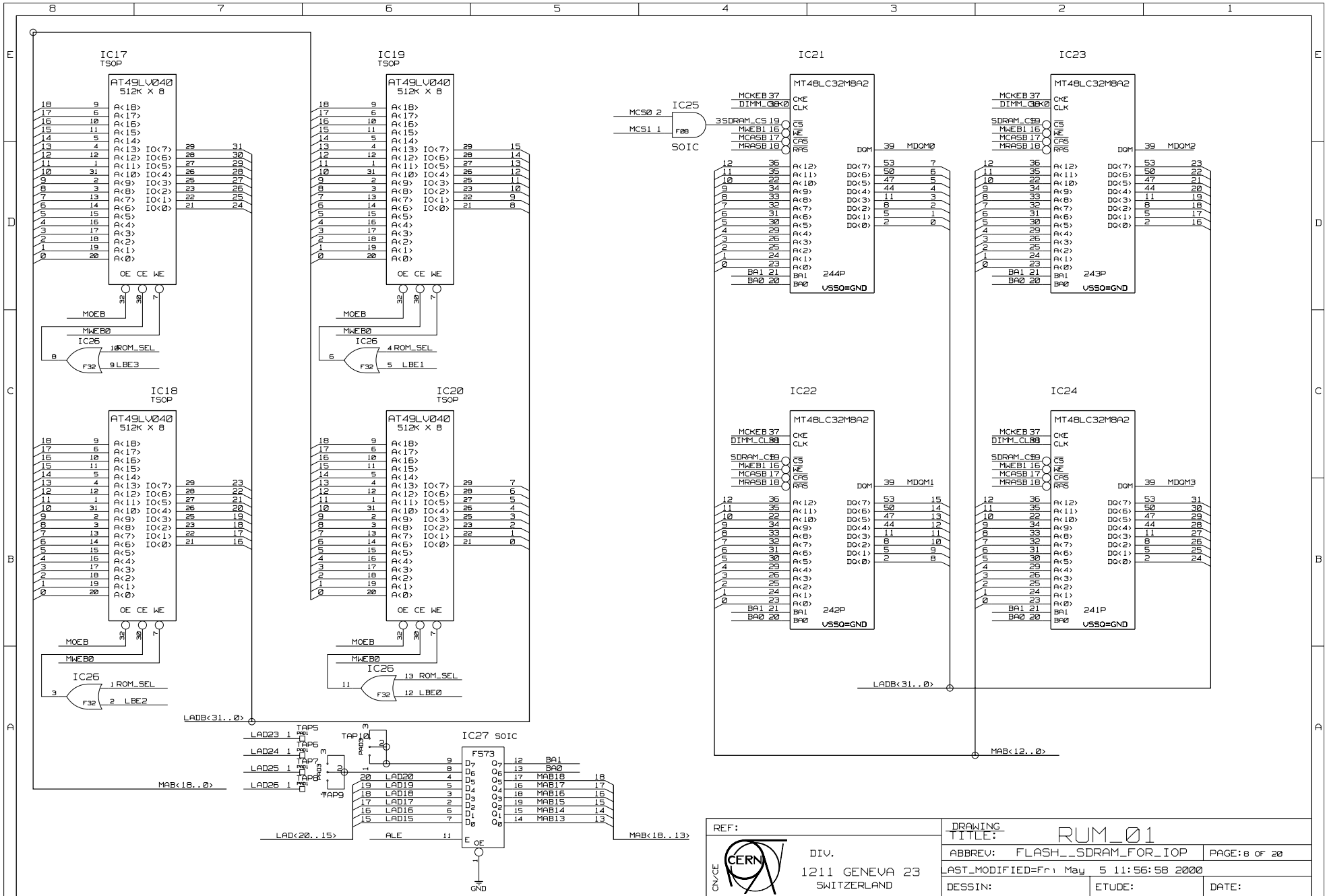
REF:	CMS DAQ GROUP DIV. EP/CMD 1211 GENEVA 23 SWITZERLAND	DRAWING TITLE:	RUM_01
		ABBREV: CONNECTOR_TO_RUIO	PAGE: 5 OF 20
		LAST_MODIFIED=Fri May 5 11:55:39 2000	
		DESSIN:	ETUDE: DATE:

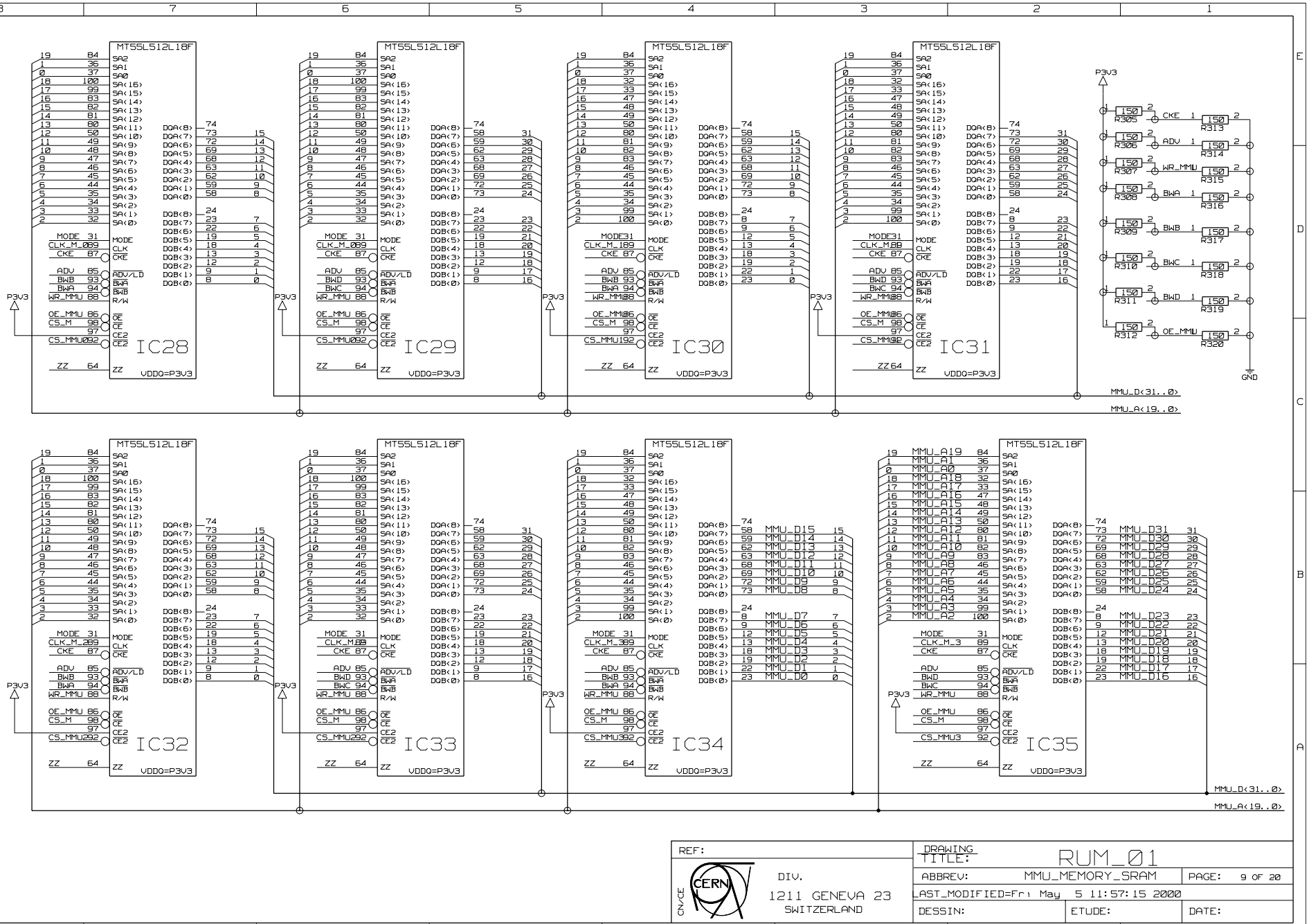

CHAIN A TDI_A5----->TDO_A
IC7 LQFP
INTEL 21143
EEP_DO_ETH
IC6 SOIC
NM93CS66
EEP_DI_ETH
EEP_CS_ETH
EEP_CLK_ETH
P3V3
5.1K R145
5.1K R146
GND
IC65
F04
POWER_DOWN
25MHZ
PHY_RESET
IC9
PACK_TYPE=TQFP
QS6611
TX+
TX-
RX+
RX-
PHY_TX+
PHY_TX-
PHY_RX+
PHY_RX-
C48
C49
1.0NF
10RX+
10RX-
SEL10_100
RZ65 135P
RZ53
RZ54
RZ55
10K
4K7 R167
100DET
DCRBP
M3/NRZIBP
DLOCK
TP3
TP4
IC11 SOIC
LD2 TIL271
LD1 HLMP6400
LED0
LED1
1K R168
1K R169
51 R159
51 R160
75 R158
75 R157
1UF C10
78P
75P
1UF C7
CLK_20_OUT
MII_RCLK
MII_TCLK1
IC10 PACK_TYPE=SOIC
TG110 S050N2
J13
RJ45SM
HOLE1
HOLE2
AGND
100 R172
120 R170
51 R173
100 R174
22 R175
100 R171
22 R176
C16 100NF
C17 100NF
75 R177
75 R178
75 R179
75 R180
C18 1NF
IDSEL
2K2 R147
C11 22NF
RESET_CTRL
GNT0_M
ETHE_PCLK
TMS_A
TCK_A
TDI_A5
10RX-
10RX+
EEP_DO_ETH
CLK_20_OUT
IC8 IQXO70 20MHZ
EN/D OUT
75 R148
25MHZ
REF:
DIV.
1211 GENEVA 23
SWITZERLAND
CERN
DRAWING TITLE: RUM_01
ABBREV: ETHERNET_CONTROLLER
PAGE: 6 OF 20
LAST_MODIFIED=Fri May 5 11:55:59 2000
DESSIN:
ETUDE:
DATE:



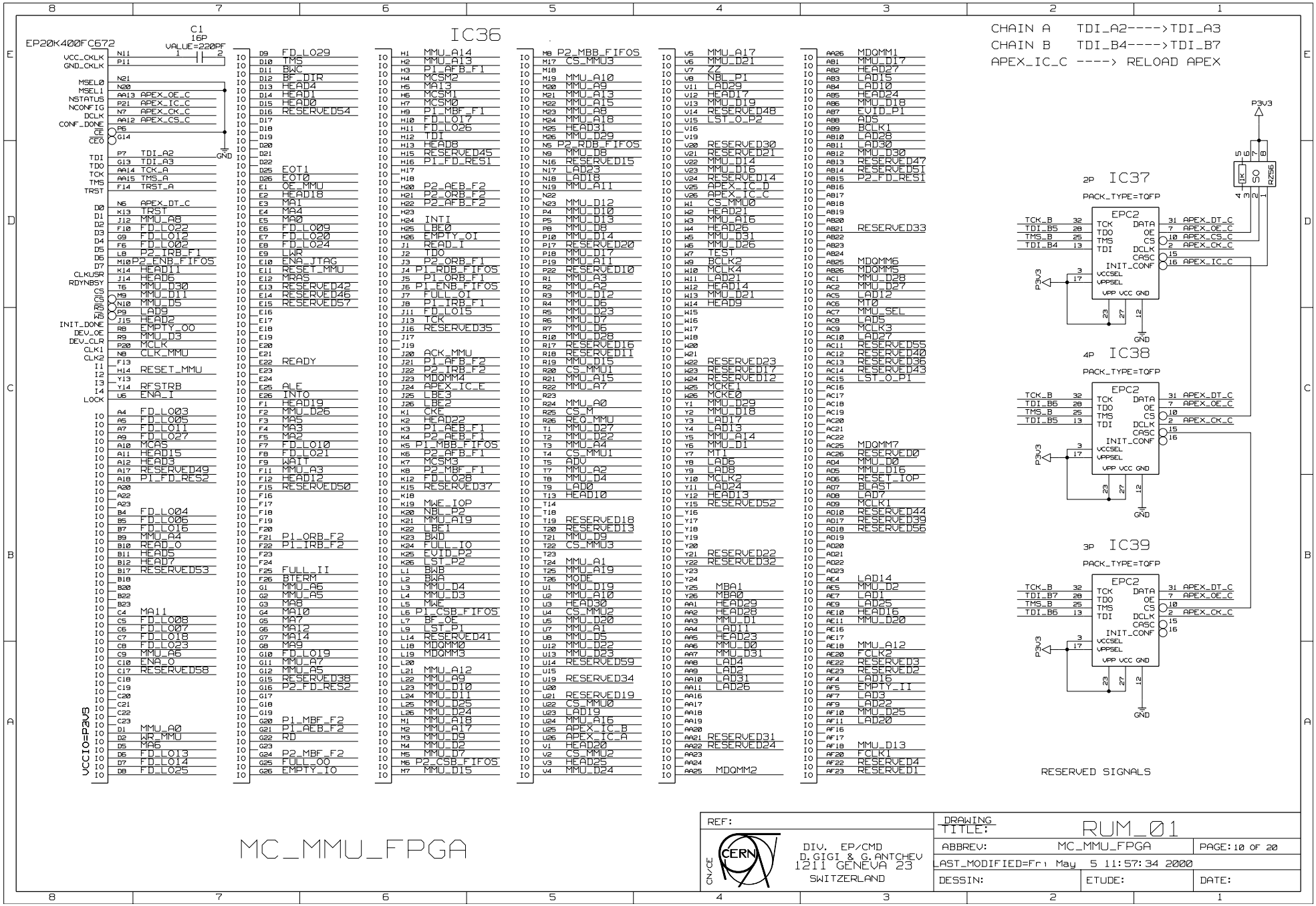
LOCAL BUS BUFFERS

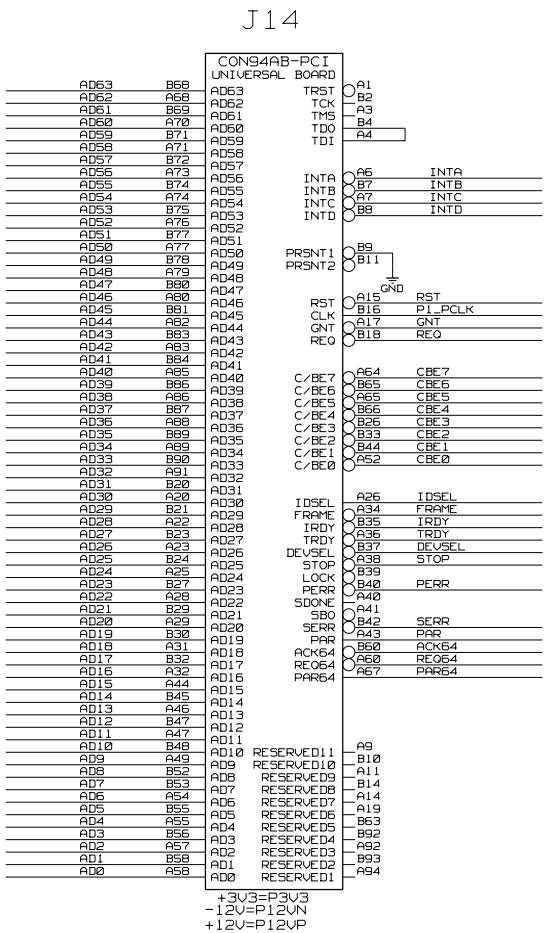
REF:	DRAWING TITLE: RUM_01	
CERN / CN-CE DIV. EP/CMD D.GIGI & G.ANTCHEV 1211 GENEVA 23 SWITZERLAND	ABBREV: LOCAL_BUS_BUFFER	PAGE: 7 OF 20
	LAST_MODIFIED=Fri May 5 11:56:14 2000	
	DESSIN:	ETUDE: DATE:

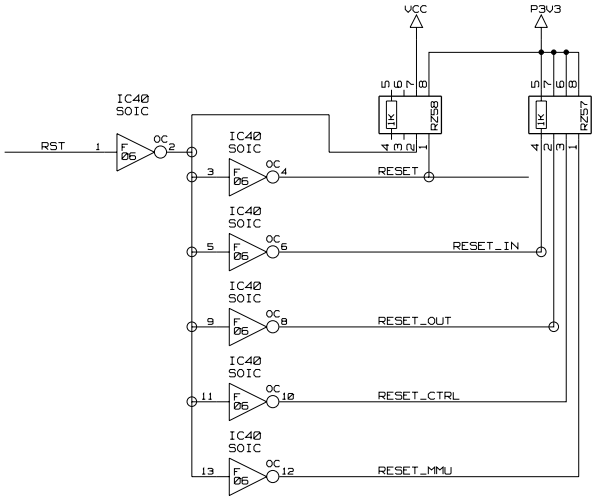

IC17
TSOP
AT49LV040
512K X 8
IC19
TSOP
AT49LV040
512K X 8
IC18
TSOP
AT49LV040
512K X 8
IC20
TSOP
AT49LV040
512K X 8
IC21
MT48LC32M8A2
244P
IC23
MT48LC32M8A2
243P
IC22
MT48LC32M8A2
242P
IC24
MT48LC32M8A2
241P
IC25
SOIC
F08
IC26
F32
IC27 SOIC
F573
MOEB
MWEB0
ROM_SEL
LBE3
LBE1
LBE2
LBE0
LADB<31..0>
MAB<18..0>
MAB<12..0>
LAD<20..15>
MAB<18..13>
ALE
GND
VSSQ=GND
REF:
DIV.
1211 GENEVA 23
SWITZERLAND
DRAWING TITLE:
RUM_01
ABBREV: FLASH__SDRAM_FOR_IOP
PAGE:8 OF 20
LAST_MODIFIED=Fri May 5 11:56:58 2000
DESSIN:
ETUDE:
DATE:



REF:	DRAWING TITLE: RUM_01	
CERN DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: MMU_MEMORY_SRAM	PAGE: 9 OF 20
	LAST_MODIFIED=Fri May 5 11:57:15 2000	
	DESSIN:	ETUDE: DATE:


EP20K400FC672
C1
16P
VALUE=220PF
IC36
CHAIN A TDI_A2----->TDI_A3
CHAIN B TDI_B4----->TDI_B7
APEX_IC_C ----> RELOAD APEX
P3V3
2P IC37
PACK_TYPE=TQFP
4P IC38
PACK_TYPE=TQFP
3P IC39
PACK_TYPE=TQFP
EPC2
RESERVED SIGNALS
MC_MMU_FPGA
REF:
DIV. EP/CMD
D.GIGI & G.ANTCHEV
1211 GENEVA 23
SWITZERLAND
DRAWING TITLE: RUM_01
ABBREV: MC_MMU_FPGA
PAGE: 10 OF 20
LAST_MODIFIED=Fri May 5 11:57:34 2000
DESSIN:
ETUDE:
DATE:





CONTROL PCI BUS SPECIFICATION

REQ / GNT

REQ0_M/GNT0_M EHTERNET
REQ1_M/GNT1_M BRIDGE RUM MMU
REQ2_M/GNT2_M PMC DEBUGGER

IDSEL

AD16_M ---> IOP480
AD17_M ---> ETHERNET
AD18_M ---> PMC DEBUGGER

INPUT PCI BUS SPECIFICATION

REQ / GNT

REQ0_I/GNT0_I PMC RUI
REQ1_I/GNT1_I PCI RUI
REQ2_I/GNT2_I PMC RUM
REQ3_I/GNT3_I PCI DATA IN
REQ4_I/GNT4_I BRIDGE RUI
REQ5_I/GNT5_I BRIDGE RUM IN

IDSEL

AD16_I ---> PMC RUI
AD17_I ---> PCI RUI
AD18_I ---> PCI DATA IN
AD19_I ---> PMC RUM

OUTPUT PCI BUS SPECIFICATION

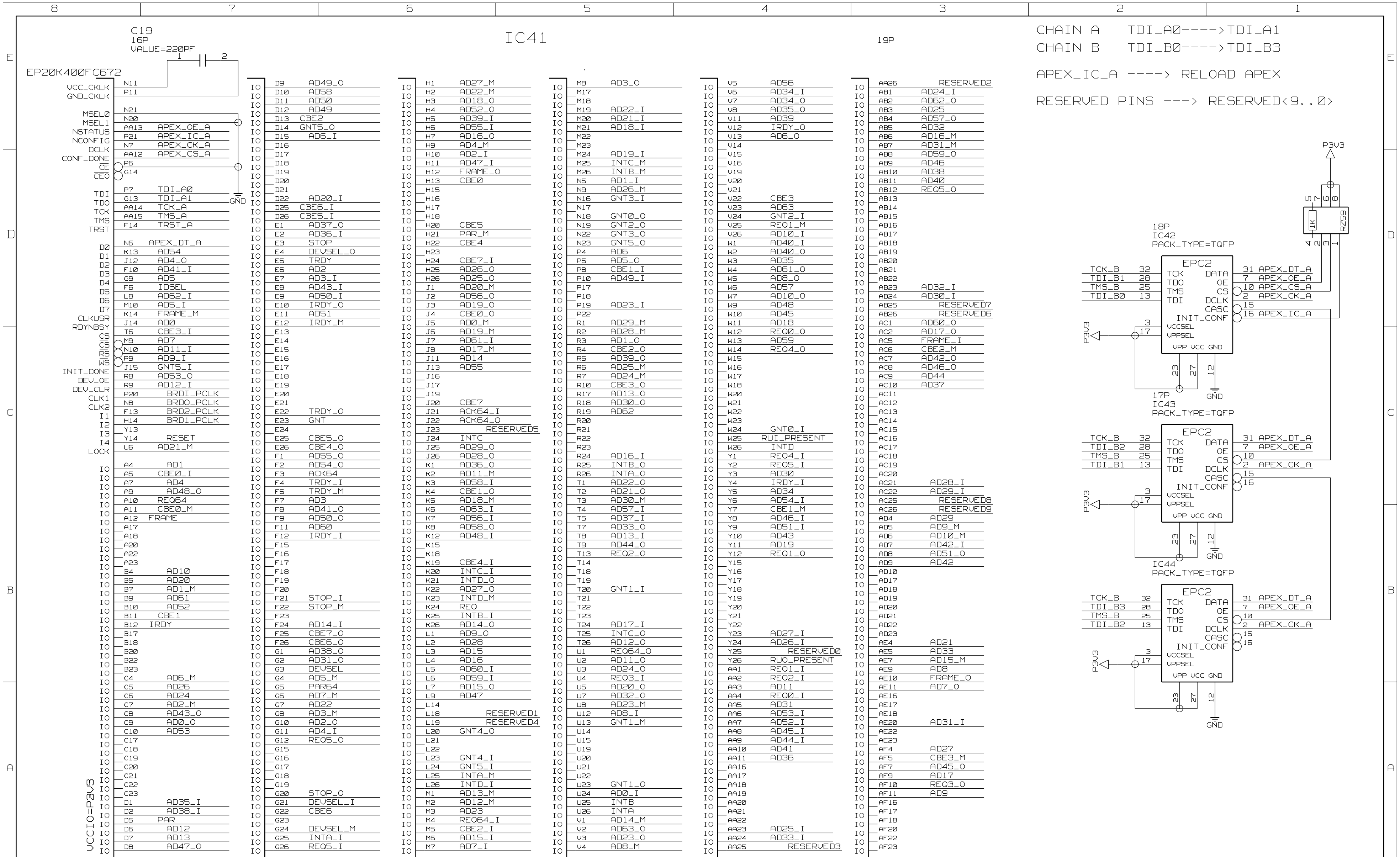
REQ / GNT

REQ0_O/GNT0_O PMC RUO
REQ1_O/GNT1_O PCI RUO
REQ2_O/GNT2_O NOT USED
REQ3_O/GNT3_O PCI DATA OUT
REQ4_O/GNT4_O BRIDGE RUO
REQ5_O/GNT5_O BRIDGE RUM OUT

IDSEL

AD16_O ---> PMC RUO
AD17_O ---> PCI RUO
AD18_O ---> PCI DATA OUT

REF:	DRAWING TITLE: RUM_01	
CERN DIV. 1211 GENEVA 23 SWITZERLAND	ABBREV: PRIMARY_PCI_CONNECTOR	PAGE: 11 OF 20
	LAST_MODIFIED=Fri May 5 11:57:51 2000	
	DESSIN:	ETUDE: DATE:



REF:

CERN

CN/CE

DIV.

1211 GENEVA 23

SWITZERLAND

DRAWING TITLE: RUM_01

ABBREV: MAIN_PCI_BRIDGE

PAGE: 12 OF 20

LAST_MODIFIED=Fri May 5 11:58:07 2000

DESSIN:

ETUDE:

DATE:

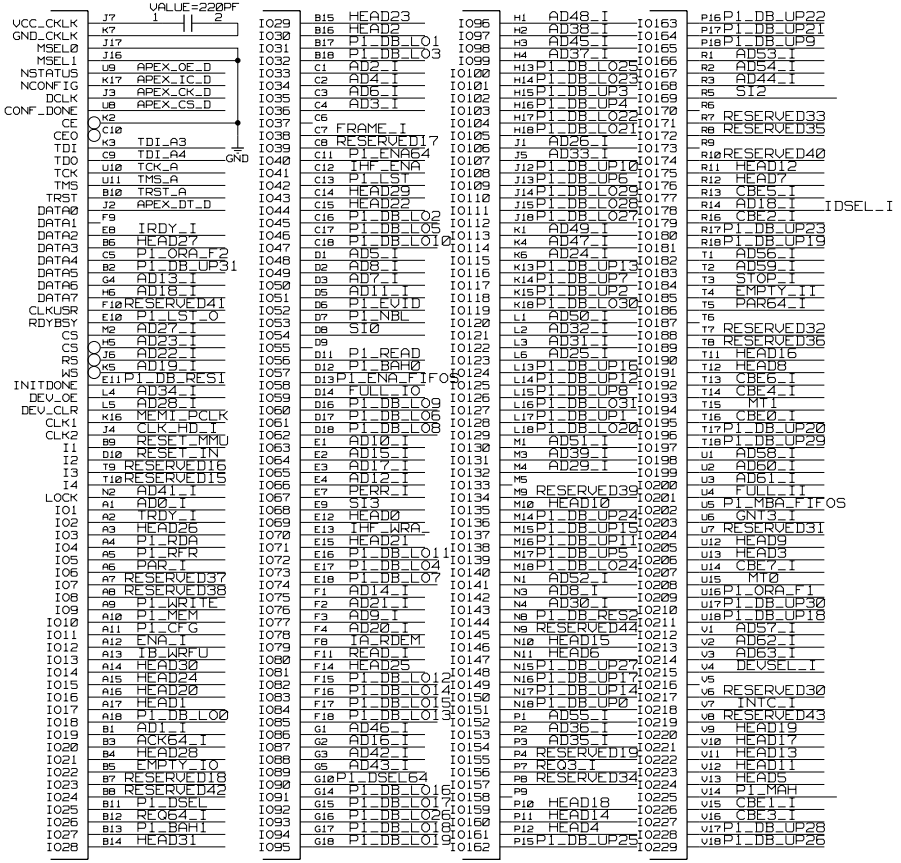
PCI INTERFACE FOR INPUT DATA

CHAIN A TDI_A3----->TDI_A4
CHAIN B TDI_B7----->TDI_B8
APEX_IC_D ----> RELOAD APEX

IC45

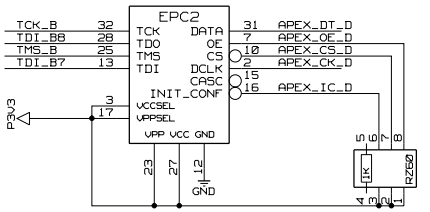
EP20K100_324

C2
10P
VALUE=220PF



IC46

PACK_TYPE=TQFP



FIFO_W/RB_ = READ_I
FIFO_ENB = ENA_I

B_RDEM = EMPTY_II
B_RDFU = FULL_II
B_WRFU = IB_WRFU

FIFO_ENA = IHF_ENA
FIFO_W/RA_ = IHF_WRA_

A_WREM = EMPTY_IO
A_WRFU = FUII_IO
A_RDEM = IA_RDEM

AD18_I = IDSEL_I

HEADER FIFO SIGNALS

RESERVED SIGNALS

PACK_TYPE=BGA
VCCIO=P3V3

VCCINT=P2V5

GNDINT=GND

REF:	DRAWING TITLE:	RUM_01
CERN DIV. EP/CMD D.GIGI & G.ANTCHEV 1211 GENEVA 23 SWITZERLAND	ABBREV: PCI_INPUT_DATA	PAGE: 13 OF 20
	LAST_MODIFIED=Fri May 5 12:01:03 2000	
	DESSIN:	ETUDE: DATE:

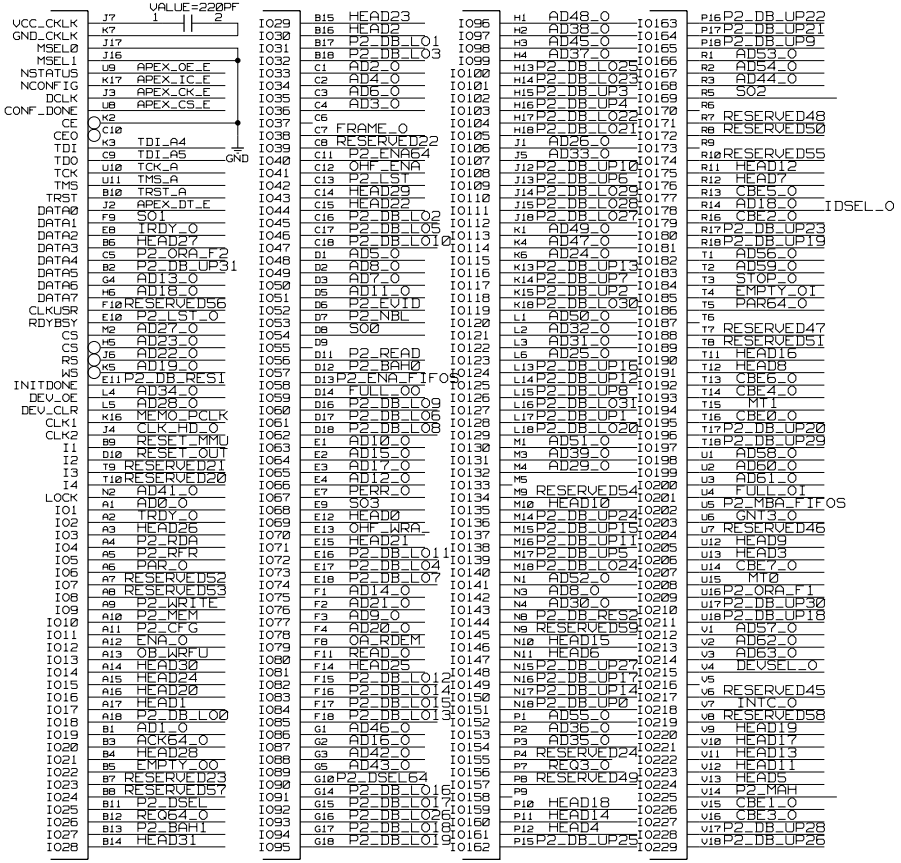
PCI INTERFACE FOR OUTPUT DATA

CHAIN A TDI_A4----->TDI_A5
CHAIN B TDI_B8----->TDO_B
APEX_IC_E ----> RELOAD APEX

IC47

EP20K100_324

C3
10P
VALUE=220PF



PACK_TYPE=BGA
VCCIO=P3V3
VCCINT=P2V5
GNDINT=GND

FIFO_W/RB_ = READ_O
FIFO_ENB = ENA_O

B_RDEM = EMPTY_OI
B_RDFU = FULL_OI
B_WRFU = OB_WRFU

FIFO_ENA = OHF_ENA
FIFO_W/RA_ = OHF_WRA_

A_WREM = EMPTY_OO
A_WRFU = FULL_OO
A_RDEM = OA_RDEM

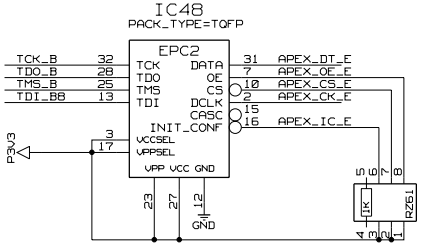
AD18_O = IDSEL_O

HEADER FIFO SIGNALS

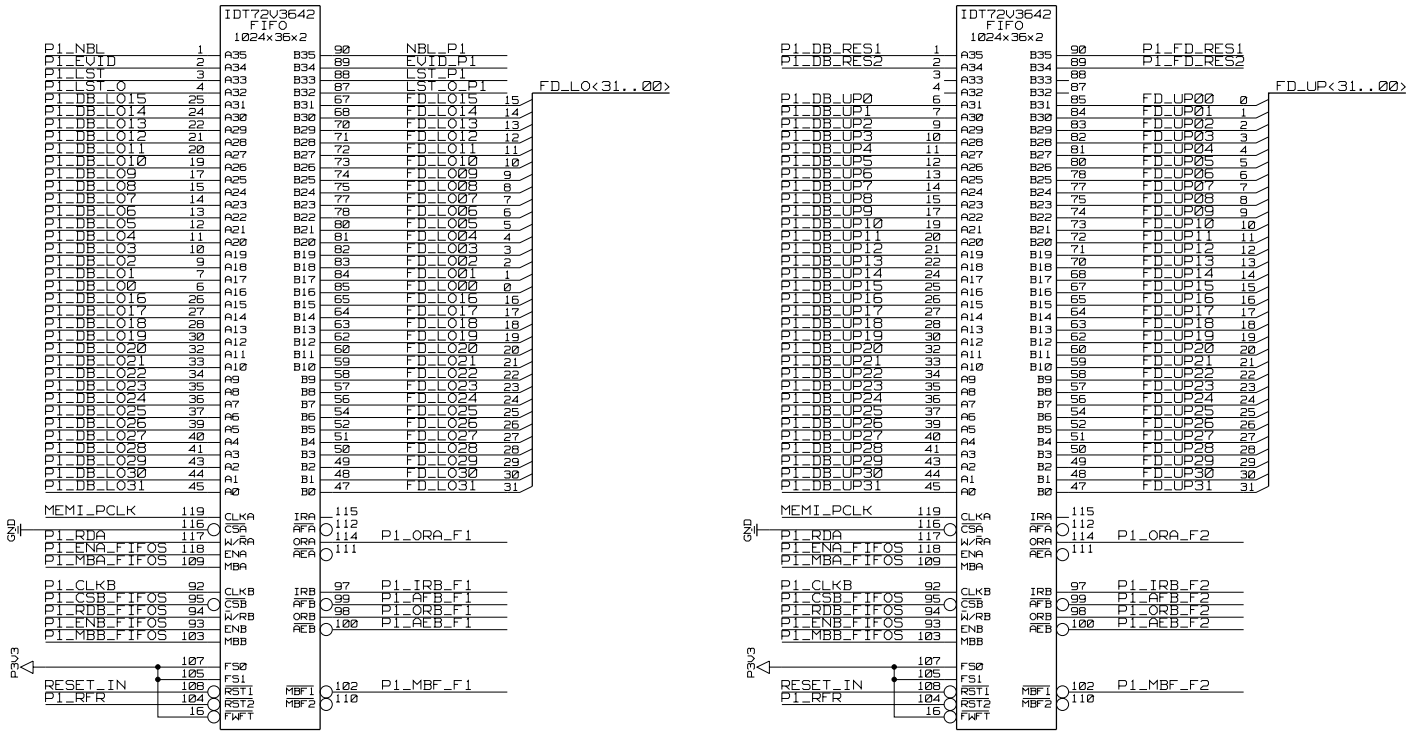
RESERVED SIGNALS

IC48

PACK_TYPE=TQFP



REF:	DRAWING TITLE: RUM_01		
CERN DIV. EP/CMD D.GIGI & G.ANTCHEV 1211 GENEVA 23 SWITZERLAND	ABBREV: PCI_OUTPUT_DATA		PAGE: 14 OF 20
	LAST_MODIFIED=Fri May 5 11:58:45 2000		
	DESSIN:	ETUDE:	DATE:



REF:

CERN CN/CE

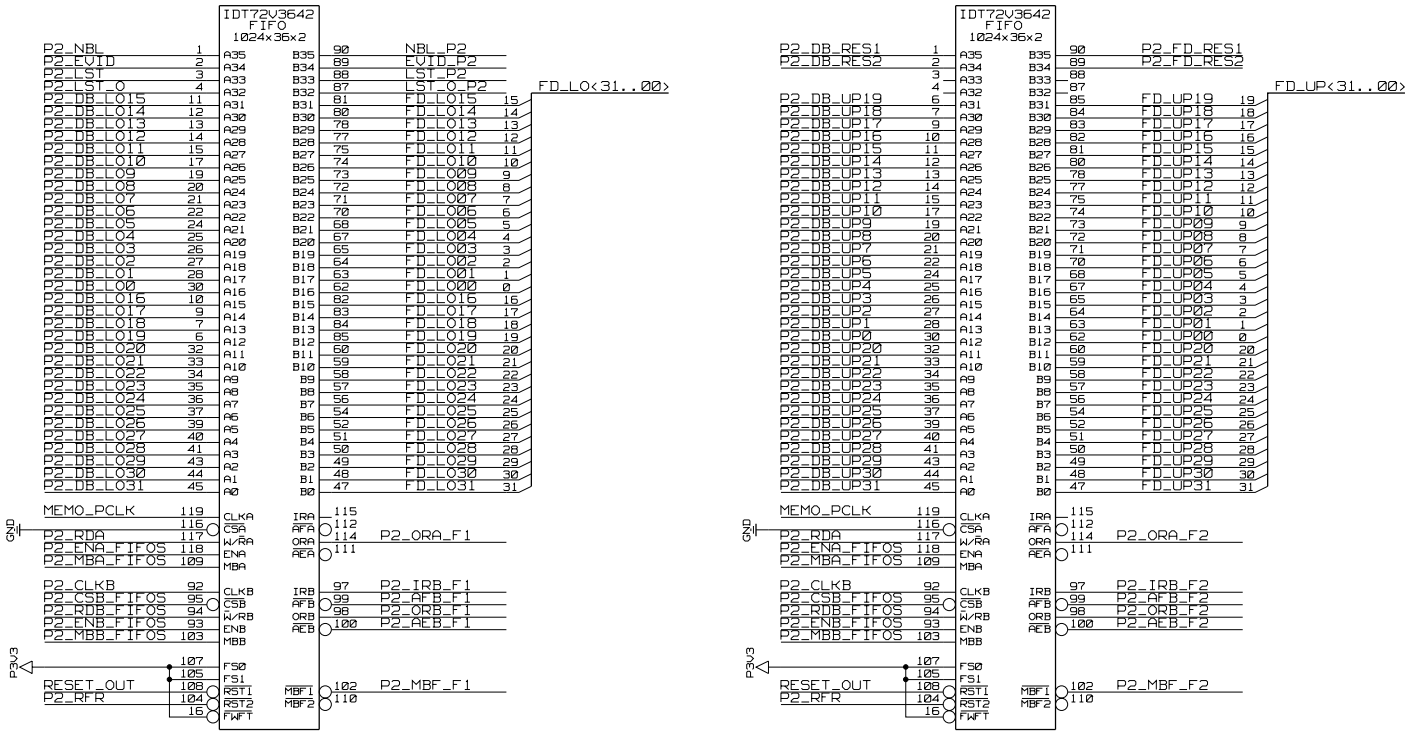
DIV. EP/CMD
D.GIGI & G.ANICHEV
1211 GENEVA 23
SWITZERLAND

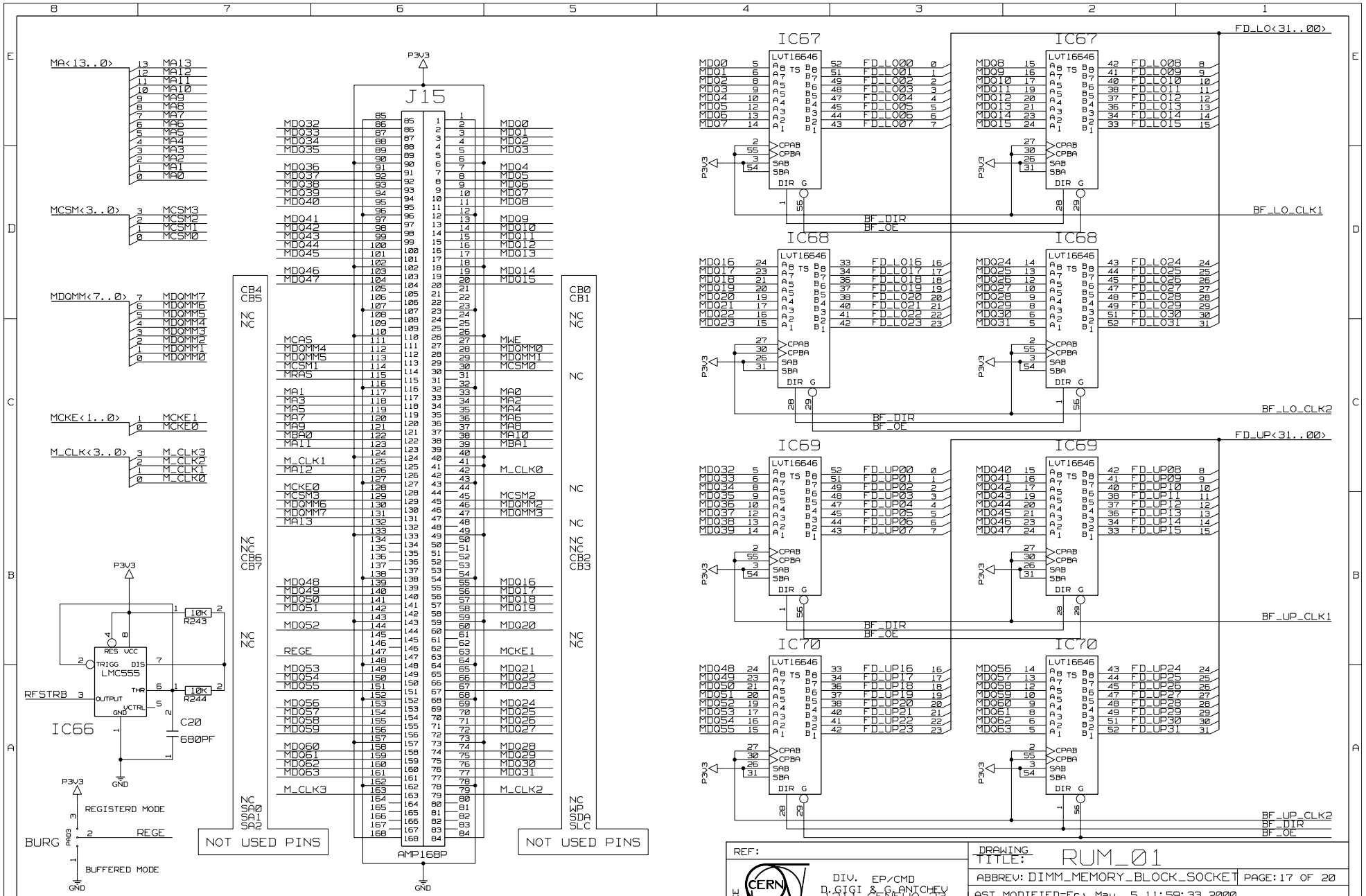
DRAWING TITLE: RUM_01

ABBREV: PORT1_INPUT_FIFO1_2 | PAGE: 15 OF 20

LAST_MODIFIED=Fri May 5 11:59:04 2000

DESSIN: | ETUDE: | DATE:


IC51
IDT72V3642
FIFO
1024x36x2
P2_NBL
P2_EVID
P2_LST
P2_LST_O
P2_DB_LO15
P2_DB_LO14
P2_DB_LO13
P2_DB_LO12
P2_DB_LO11
P2_DB_LO10
P2_DB_LO9
P2_DB_LO8
P2_DB_LO7
P2_DB_LO6
P2_DB_LO5
P2_DB_LO4
P2_DB_LO3
P2_DB_LO2
P2_DB_LO1
P2_DB_LO0
P2_DB_LO16
P2_DB_LO17
P2_DB_LO18
P2_DB_LO19
P2_DB_LO20
P2_DB_LO21
P2_DB_LO22
P2_DB_LO23
P2_DB_LO24
P2_DB_LO25
P2_DB_LO26
P2_DB_LO27
P2_DB_LO28
P2_DB_LO29
P2_DB_LO30
P2_DB_LO31
NBL_P2
EVID_P2
LST_P2
LST_O_P2
FD_LO<31..00>
MEMO_PCLK
GND
P2_RDA
P2_ENA_FIFOS
P2_MBA_FIFOS
P2_ORA_F1
P2_CLKB
P2_CSB_FIFOS
P2_RDB_FIFOS
P2_ENB_FIFOS
P2_MBB_FIFOS
P2_IRB_F1
P2_AFB_F1
P2_ORB_F1
P2_AEB_F1
P3V3
RESET_OUT
P2_RFR
P2_MBF_F1
IC52
IDT72V3642
FIFO
1024x36x2
P2_DB_RES1
P2_DB_RES2
P2_DB_UP19
P2_DB_UP18
P2_DB_UP17
P2_DB_UP16
P2_DB_UP15
P2_DB_UP14
P2_DB_UP13
P2_DB_UP12
P2_DB_UP11
P2_DB_UP10
P2_DB_UP9
P2_DB_UP8
P2_DB_UP7
P2_DB_UP6
P2_DB_UP5
P2_DB_UP4
P2_DB_UP3
P2_DB_UP2
P2_DB_UP1
P2_DB_UP0
P2_DB_UP20
P2_DB_UP21
P2_DB_UP22
P2_DB_UP23
P2_DB_UP24
P2_DB_UP25
P2_DB_UP26
P2_DB_UP27
P2_DB_UP28
P2_DB_UP29
P2_DB_UP30
P2_DB_UP31
P2_FD_RES1
P2_FD_RES2
FD_UP<31..00>
MEMO_PCLK
GND
P2_RDA
P2_ENA_FIFOS
P2_MBA_FIFOS
P2_ORA_F2
P2_CLKB
P2_CSB_FIFOS
P2_RDB_FIFOS
P2_ENB_FIFOS
P2_MBB_FIFOS
P2_IRB_F2
P2_AFB_F2
P2_ORB_F2
P2_AEB_F2
P3V3
RESET_OUT
P2_RFR
P2_MBF_F2
REF:
CERN
DIV. EP/CMD
D.GIGI & G.ANTCHEV
1211 GENEVA 23
SWITZERLAND
DRAWING TITLE: RUM_01
ABBREV: PORT2_OUTPUT_FIFO1_2
PAGE: 16 OF 20
LAST_MODIFIED=Fri May 5 11:59:18 2000
DESSIN:
ETUDE:
DATE:



DIMM SOCKET FOR 16/64/128MBIT SDRAM'S

REF:

CERN

DIV. EP/CMD
D.GIGI & G.ANICHEV
1211 GENEVA 23
SWITZERLAND

DRAWING TITLE: RUM_01

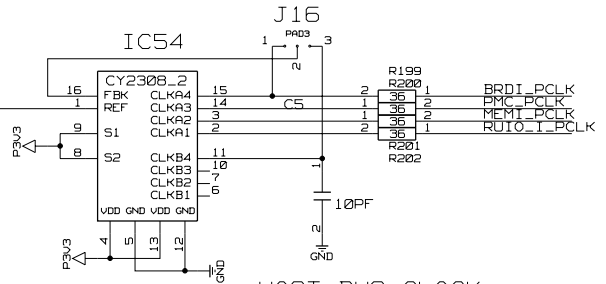
ABBREV: DIMM_MEMORY_BLOCK_SOCKET | PAGE: 17 OF 20

LAST_MODIFIED=Fri May 5 11:59:33 2000

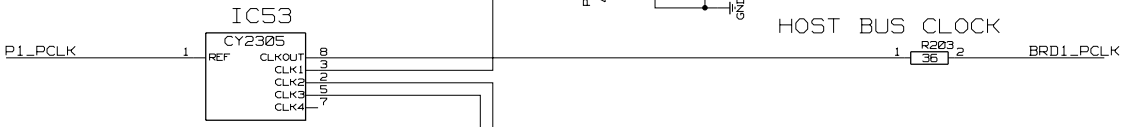
DESSIN: | ETUDE: | DATE:

DISTRIBUTION OF PCI CLOCK 33/66MHZ

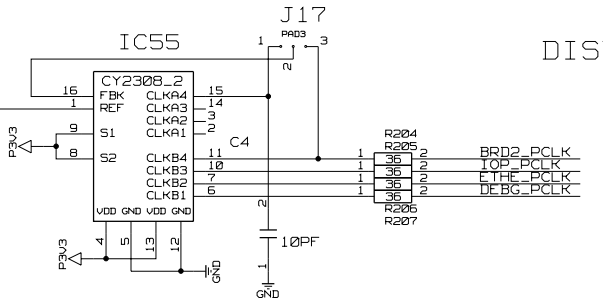
PCI INPUT BUS CLOCK'S



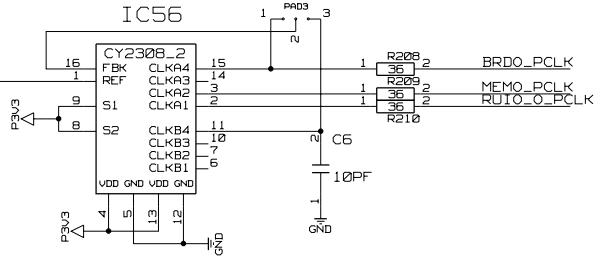
HOST BUS CLOCK



PCI CONTROL BUS CLOCK



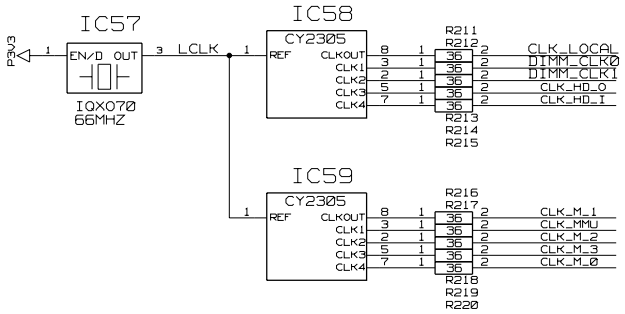
PCI OUTPUT BUS CLOCK'S



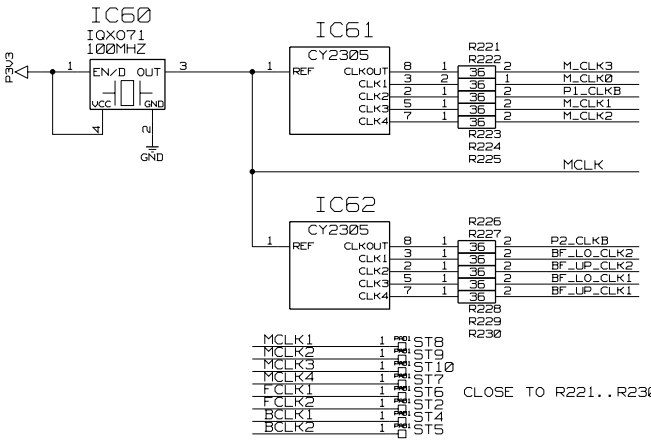
PRIMARY BUS	33MHZ	66MHZ
INPUT BUS		
J16 33MHZ	1-2	NP
J16 66MHZ	2-3	1-2
OUTPUT BUS		
J18 33MHZ	1-2	NP
J18 66MHZ	2-3	1-2
MMU BUS		
J17 33MHZ	2-3	1-2

CLOSE CONNECTION X-X
NP = NOT PERMITTED

DISTRIBUTION OF LOCAL CLOCK 66MHZ

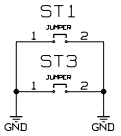


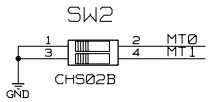
DISTRIBUTION OF DIMM/FIFO CLOCK 100MHZ



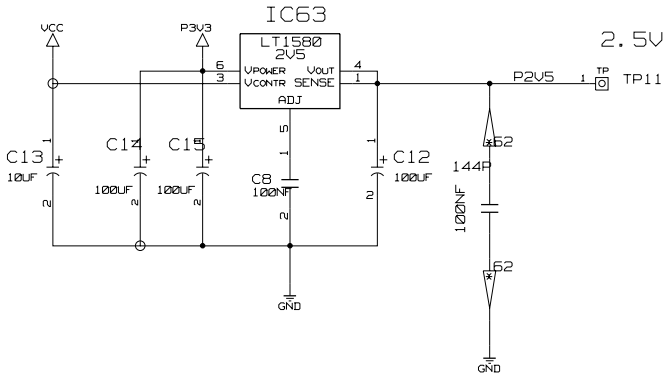
REF:	DRAWING TITLE: RUM_01		
CERN / CN-CE — DIV. EP/CMD, G.GIGI & G.ANTCHEV, 1211 GENEVA 23, SWITZERLAND	ABBREV: CLOCKS_BLOCK		PAGE: 18 OF 20
	LAST_MODIFIED=Fri May 5 11:59:48 2000		
	DESSIN:	ETUDE:	DATE:

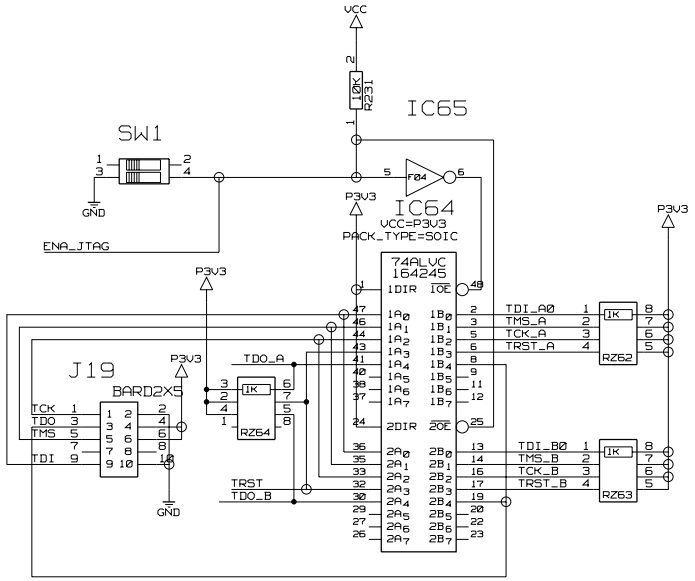
DECOUPLING FOR 3.3V / 5V



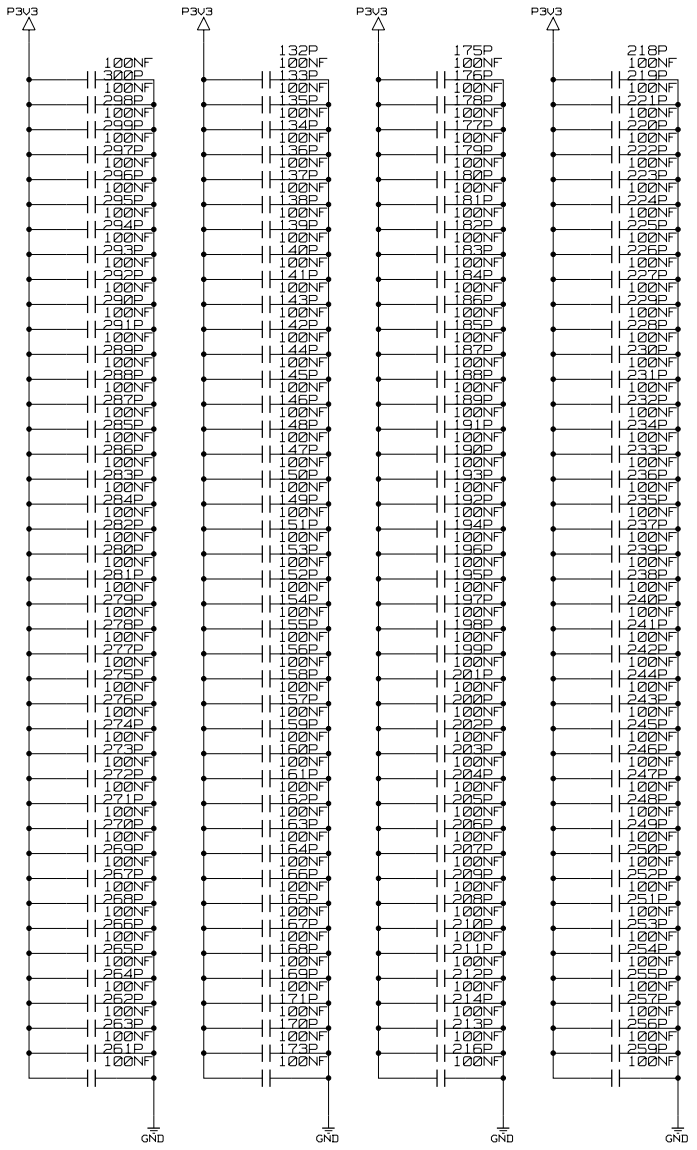


ALTERA CORE SUPPLY 2.5V





REF:	DRAWING TITLE: RUM_01	
CERN / DIV. EP/CMD / D.GIGI & G.ANICHEV / 1211 GENEVA 23 / SWITZERLAND	ABBREV: POWER_JTAG_BLOCK	PAGE: 19 OF 20
	LAST_MODIFIED=Fri May 5 12:00:05 2000	
	DESSIN:	ETUDE: DATE:



REF:	DRAWING TITLE:	RUM_01	
CERN / DIV. EP/CMD / D.GIGI & G.ANICHEV / 1211 GENEVA 23 / SWITZERLAND	ABBREV:	CAPACITORS_PAGE	PAGE: 20 OF 20
	LAST_MODIFIED=Fri May 5 12:00:46 2000		
	DESSIN:	ETUDE:	DATE: