TOTEM	TOTEM Experiment COINCIDENCE CHIP SPECIFICATION		
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TOTEM COINCIDENCE CHIP SPECIFICATION

Abstract

This document provides the full specification of the TOTEM coincidence chip, the CC chip. This chip will act on fast trigger signals generated by the detectors' front ends to establish coincidence between different detector planes to establish that a certain number of tracks traversed the detector. In addition the chip will impose some multiplicity constraints to verify whether the event for which particle tracks were detected is sufficiently interesting to generate a level 1 trigger for its readout. This chip is the basis for the generation of the trigger signals provided by TOTEM to the CMS global trigger.

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1 Introduction

The detector front ends in TOTEM generate fast signals which are used to generate the trigger signals provided by TOTEM to the CMS global trigger box. We have opted for the development of a full custom chip rather than using a Field Programmable Gate Array for two main reasons:

1. The latency constraints on the generation of the trigger bits especially from the Roman Pots are very severe: after subtraction of cable delays only about 8-10 bunch crossings are left for the generation of the trigger signals to be provided to CMS from the signals generated by the Roman Pot detector front end. A full custom chip with dedicated logic can implement the required coincidence in one clock cycle, while an FPGA will typically need more time because it was conceived to be much more versatile.
2. Special design techniques can make a full custom chip much more robust against radiation both with regard to total dose and single event effects. This allows to place this chip in aggressive radiation environments very near the detectors. This has the non-negligible advantage that the number of signals is very severely reduced prior to carrying these signals away from the detector, which presents considerable space and cost savings. (Note that the CC chip will be submitted together with the VFAT chip for a very limited marginal cost).

Some programmability of the CC chip is required to deal with different detector geometries and evaluate trigger efficiencies. This programmability is achieved through the use of an I2C interface which makes the CC chip compatible with the standard CMS tracker and ecal control system. This system will also control the VFAT and APV used within the TOTEM experiment and therefore this was the most cost-effective way to obtain programmable trigger generation hardware.

2 Architecture

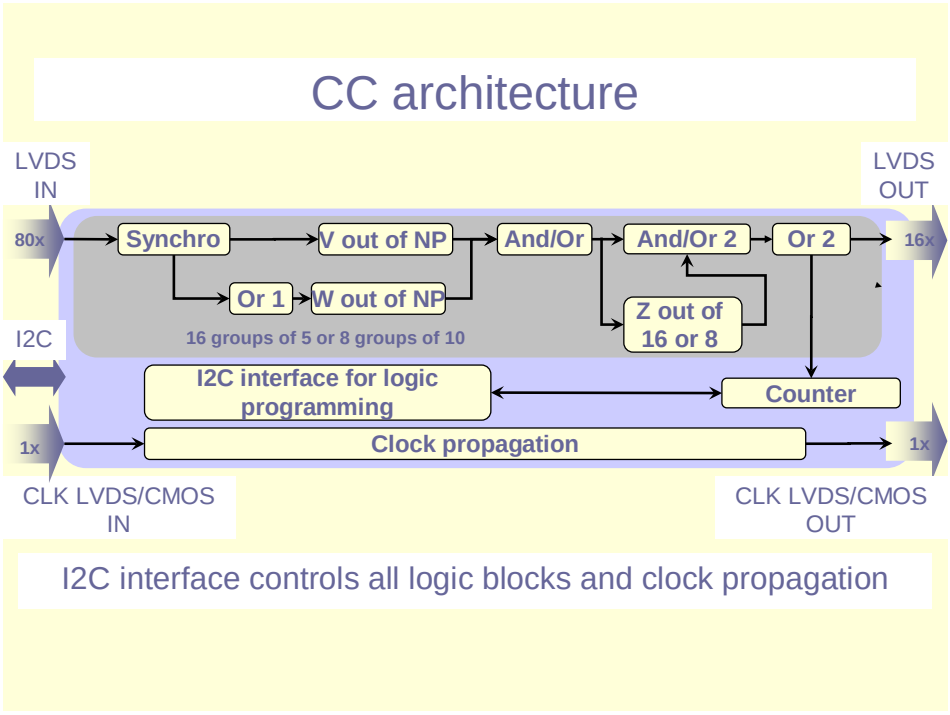

Fig. 1. General CC architecture.

Fig. 1 shows the general CC architecture. The VFAT sends LVDS signals to avoid coupling of digital signals into the analog front end. The CC chip receives 80 digital LVDS inputs which it converts into CMOS on chip. To do the impedance matching, all of the 80 digital LVDS inputs have a programmable resistance (chapter 5). These 80 digital signals normally correspond to a certain number of coordinates or sectors on a certain number of detector planes. To establish that a real particle track passed through the detector, coincidence will be required between detector planes in corresponding coordinates. To accommodate detectors with various reaction times and jitter within the detector synchronization maybe required. There is a synchronization module per input channel which can be programmed to stretch a pulse over a number of clock cycles and/or to synchronize the pulse with the clock.

For flexibility the number of detector planes between which coincidence will be required is programmable. To implement this, the inputs are grouped as illustrated in fig. 2. The maximum number of planes is fixed at 10. If the number of planes is 5 or less, the inputs will be grouped in groups of 5 each of which will correspond to a certain coordinate on the different detector planes between which coincidence will be required. If the number of planes is 5 all inputs in a group will be used, if the number is less, the last input or inputs in each group will not be used, and will be disabled internally to avoid errors due to floating inputs. In addition high-value resistors are used to avoid arbitrary floating of non-used inputs.

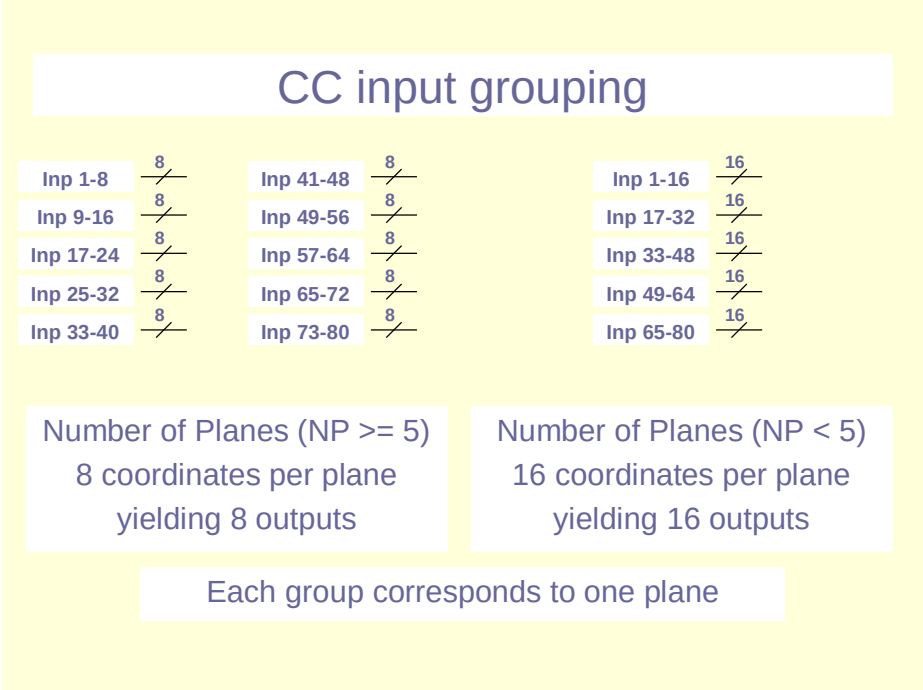

Fig. 2. General organization of the inputs of the CC chip.

If the number of planes to be put into coincidence is greater than 5, the inputs will be grouped in groups of 10, possibly with the last ones unused for a number of planes less than 10. This choice of creating groups of inputs has been made as a compromise between on-chip interconnect complexity and efficient use of inputs: allowing grouping of inputs in a fully arbitrary way would result in very complex interconnect; having two modes of grouping makes the use of the chip more efficient for a small number of detector planes.

The number of planes is specified is specified in the I2C register NP.

Now the different programmable logic blocks in the CC will be detailed:

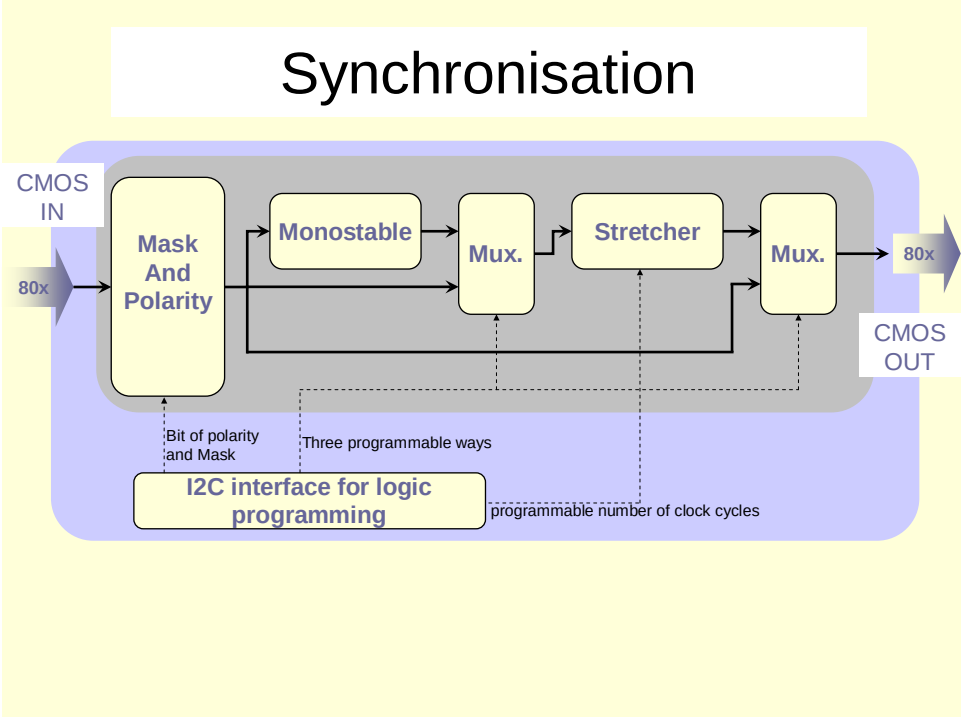

fig. 3. Synchronisation architecture

The input signals are first converted from LVDS to CMOS, they are **masked or not** and their **polarity is changed or not** depending on the setting of the registers controlling this. The polarity is defined for all signals at the same time (so only one bit per chip (the LI register)) while every channel can be masked individually. After this the signals are treated by their synchronization blocks. The synchronization block for every channel contains a circuit which transforms an incoming pulse of arbitrary length into a pulse synchronized with the clock with a length of one cycle (monostable), and a circuit which can stretch the pulse over a programmable number of cycles, again synchronized with the clock. Three modes of operation exist: either the synchronization is included completely in the signal path, or only the monostable is bypassed, or the synchronization is disabled completely. In the latter two cases it is strongly recommended to have synchronous inputs.This is controlled by the sync bits:

Sync2	*Sync*	Resulting function for Sync
0	*0*	*Stretch without Monostable*
0	*1*	*Monostable and stretcher*
1	*0*	*Only mask and polarity*
1	*1*	*Not used*

Table 1. Definition of the three input ways controlled by the Sync register

A first coincidence is carried out in the **V out of NP** block. For every group of inputs a coincidence signal will be generated requiring at least V out of the number of planes (NP) to be “on” in the corresponding coordinate. V should be specified less or equal to NP. If larger the coincidence result will always be zero. V is specified in the I2C register V.

To account for non-perfect alignment between detector planes and particles which traverse the detector at some angle another coincidence is carried out by the W out of NP block. The signals presented to this block are the result of an OR (**OR 1**) of the corresponding coordinate in a detector plane with a certain number of its nearest neighbors

specified by OV. For instance if OV equals one, each coordinate will be “or-ed” with the input corresponding to the same plane of the previous group of inputs and with the input corresponding to the same plane of the next group of inputs. So, for instance, for NP equal to 5, the or signal corresponding to input 6 will be the or of input 1, input 6, and input 11. At the edges the or will be carried out only on the available neighbour signals (so for input 1 only input 1 and input 6 will be “or-ed”). OV can be maximum 8 and is specified in the I2C register OV.

The result of this OR 1 is presented to the coincidence block **W out of NP.** Allowing some overlap gives margin for tracks at a small angle, some misalignment between planes, etc… Similar to the V out of NP block, W should be specified less or equal to NP. If larger the coincidence result will always be zero. W is specified in the I2C register W.

The result of these two coincidence blocks V out of NP and W out of NP will then be combined in the **And/Or** block. They can be ored, anded, or only one of the two can be considered. Which of these is carried out is determined by the I2C register AO.

AO 1	AO 0	Resulting function for And/Or
0	0	(V out of NP) and (W out of NP) (default)
0	1	(V out of NP) or (W out of NP)
1	0	V out of NP
1	1	W out of NP

Table 2. Definition of the function controlled by the AO register.

The **OR 2** block will combine the 16 or 8 outputs into a lesser number, if so desired: once coincidence has been established it is not always needed to have very detailed coordinate or sector information. Therefore it is possible to or sectors in groups of 2, 4 or 8. In that case only the output corresponding to the first output of the group will be active. The other outputs will be powered down to save power in the LVDS buffers. (specify whether they need to be bonded or can be left unconnected !!!). The operation of the OR 2 block is controlled by the I2C register O2.

O2 2	O2 1	O2 0	Resulting function for Or 2
0	0	0	Output all outputs (default)
0	0	1	Group outputs in groups of 2
0	1	0	Group outputs in groups of 4
0	1	1	Group outputs in groups of 8
1	0	0	Group outputs in groups of 16

Table 3. Definition of the function controlled by the O2 register.

The **Z out of 8 or 16** coincidence block provides a multiplicity criterion: if more than Z groups out of 8 or 16 depending on the mode of the circuit are active, the trigger outputs can be masked, or it can be used as another condition. The I2C register LO controls which function is implemented in the **And/Or 2 block**. The block can also be configured to invert the outputs.

LO 1	LO 0	Resulting function for And/Or 2
0	0	Output and not(Z out of 8 or 16) (default)
0	1	Output and (Z out of 8 or 16)
1	0	Not(Output and not(Z out of 8 or 16))
1	1	Not(Output and (Z out of 8 or 16))

Table 4. Definition of the function controlled by the LO register.

Similarly the I2C register LI controls whether the inputs are inverted or not.

LI	Resulting function for the inputs
0	Inputs not inverted (default)
1	Inputs inverted

Table 5. Definition of the function controlled by the LI register.

To avoid problems with noisy channels it is possible to mask every input individually. This requires 10 8 bit registers (see below).

A counting feature has been provided to be able to look at rates on every CC output. For this purpose a counter is implemented which can be read using I2C, and which can be programmed to count the number of pulses on any of the outputs. The 4 bit register CO defines which output is being counted. Counting is carried out continuously, and the CT register controls the counting period in number of clock cycles. At the end of every counting period the counting result is stored into a set of I2C registers, and a new counting period is started with a counter reset.

CT(1)	*CT(0)*	Counter Reset
0	*0*	*256*
0	*1*	*65536*
1	*0*	*16777216*
1	*1*	*4294967296*

Table 6.Definition of the Counter Reset moment controlled by the CT registers

3 Propagation path for the Clock

The CC chip will be used close to the detector but also at a few meters away. This creates a synchronization issue and requires the cable delay to be taken into account by the clock applied to the CC chip. A straight forward way to take this delay into account is to have the clock propagate in an identical way as the signals. Therefore a path for the clock is foreseen on the CC chip so that the signal shape can be restored for further propagation. The I2C register CL determines whether the input signals are sampled and evaluated during the rising or falling edge of the clock. The data will become available at the outputs a few gate delays after the clock edge used for evaluation.

CL	Definition of the evaluation moment
0	Evaluation on rising edge of CLK (default)
1	Evaluation on falling edge of CLK

Table 7. Definition of the evaluation moment controlled by the CL register.

4 Organization of the I2C registers

The previous section defined how the I2C registers influence the logic function of the chip. Here we organize these registers in groups of 8, which is the standard format for I2C. Four eight bit I2C registers fully control the logic function implemented by the CC chip. The following figure gives an overview:

register name	Bit position	7	6	5	4	3	2	1	0	mode
Control register 0	Bit control	-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S(0)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function			Counter timing			Stretcher or not		Sleep or not	
Control register 1	Bit control	OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Number of coordinates neighbors			group 5 or 10	Reference of the V out of NP block				
Control register 2	Bit control	Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)	R/W
	Sleep setting	1	1	1	1	0	0	0	0	
	Function	Reference of the Z out of 16 or 8 block				Reference of the W out of NP block				
Control register 3	Bit control	AO(2)	AO(1)	LO(1)	LO(0)	LI(0)	O2(2)	O2(1)	O2(0)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Function for And/Or		Function for And/Or		inverted inputs	Function for Or2			
Control register 4	Bit control	CL(0)	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	evaluation edge	timing of counter reset			Address of which output is being counted				
Control register 5	Bit control	Chip ID(7)	Chip ID(6)	Chip ID(5)	Chip ID(4)	Chip ID(3)	Chip ID(2)	Chip ID(1)	Chip ID(0)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Chip Identification								
Control register 6	Bit control	Chip ID(15)	Chip ID(14)	Chip ID(13)	Chip ID(12)	Chip ID(11)	Chip ID(10)	Chip ID(9)	Chip ID(8)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Chip Identification								
Control register 7	Bit control	Counter(7)	Counter(6)	Counter(5)	Counter(4)	Counter(3)	Counter(2)	Counter(1)	Counter(0)	RO
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Result of the counter								
Control register 8	Bit control	Counter(15)	Counter(14)	Counter(13)	Counter(12)	Counter(11)	Counter(10)	Counter(9)	Counter(8)	RO
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Result of the counter								
Control register 9	Bit control	Counter(23)	Counter(22)	Counter(21)	Counter(20)	Counter(19)	Counter(18)	Counter(17)	Counter(16)	RO
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Result of the counter								
Control register 10	Bit control	Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 11	Bit control	Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask(11)	Mask(10)	Mask(9)	Mask(8)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 12	Bit control	Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 13	Bit control	Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 14	Bit control	Extreg(7)	Extreg(6)	Extreg(5)	Extreg(4)	Extreg(3)	Extreg(2)	Extreg(1)	Extreg(0)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Extended register								
Control register 15	Bit control	Extreg(15)	Extreg(14)	Extreg(13)	Extreg(12)	Extreg(11)	Extreg(10)	Extreg(9)	Extreg(8)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Extended register								
Control register 0	Bit control	Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 1	Bit control	Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 2	Bit control	Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 3	Bit control	Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 4	Bit control	Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 5	Bit control	Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)	R/W
	Sleep setting	1	1	1	1	1	1	1	1	
	Function	Inputs Mask								
Control register 6	Bit control	-	-	-	-	-	B(2)	B(1)	B(0)	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Not used								
Control register 7	Bit control	-	-	-	-	-	-	-	-	R/W
	Sleep setting	0	0	0	0	0	0	0	0	
	Function	Not used								

Fig. 4. Organization of the I2C registers.

Control registers 7 to 9 contain the register for the counter, register 7 being the most significant. Register 5-6 contains the laser-written address.

In addition masking is provided for all inputs, 1 bit per input so 80 bits, spread over Indirect Control Registers 0-7, in ascending order of input channels.

5 Impedance matching

To do the impedance matching between the cables and the pads, a programmable resistor has been added which value is controlled by the B registers.

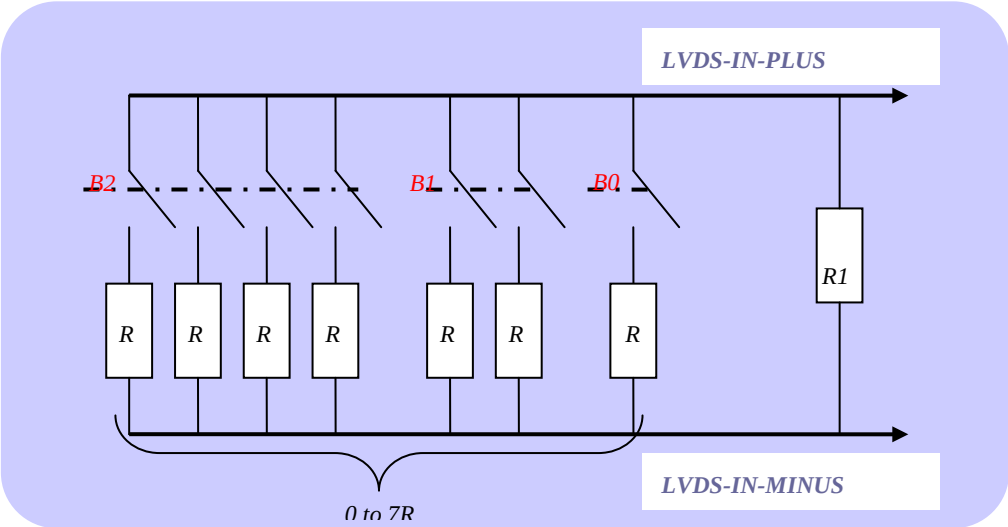

Fig.5. Resistor architecture

B2	B1	B0	Resistor(Ω)
0	0	0	126
0	0	1	115
0	1	0	105
0	1	1	97
1	0	0	90
1	0	1	84
1	1	0	79
1	1	1	74

Table 8. Value of the resistor controlled by the B registers.

6 List and organization of the pads

The inputs arrive in LVDS and are transformed into CMOS on chip. The outputs are LVDS. Figure 4 illustrates the geometry of the pad arrangement. Annex 1 provides the details.

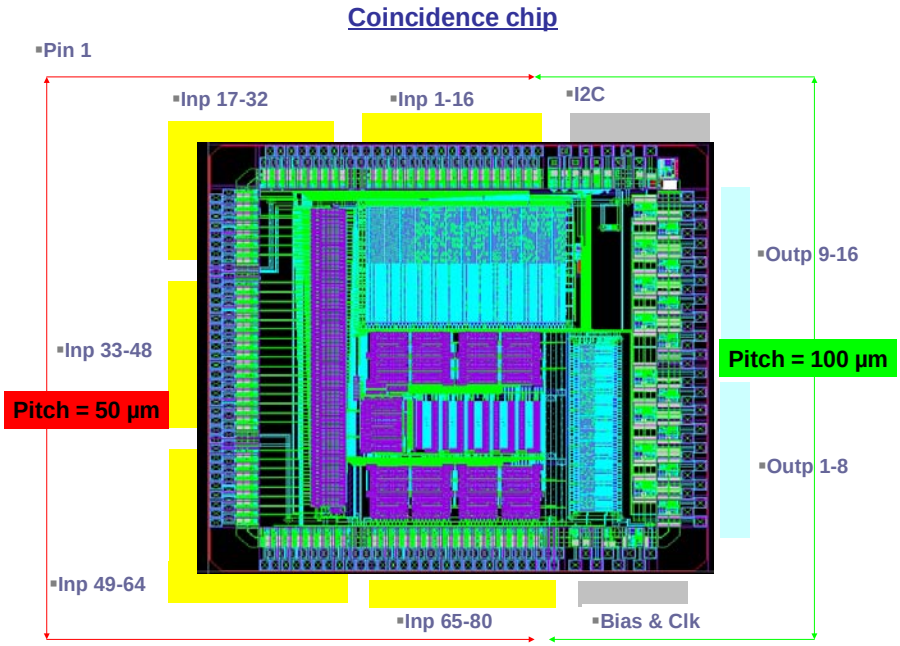

Fig. 5. Geometrical organization the pads.

7 Conclusions: benefits for the experiment

The CC chip is a chip which carries out a programmable coincidence in straight-forward way. It offers the following advantages:

1. It is radiation tolerant and can be mounted on or very near the detector, where it severely reduces the number of coincidence signals before these are sent to the counting room. For instance in the GEM it will reduce the number of bits from about 4000 to only a few (here the CC chip will be cascaded in two or three layers). For the Roman Pots two chips will be needed per pot, one for each coordinate, which reduce the number of trigger bits from 16*10 planes/pot * 6 pots = 960 to 32/pot * 6 pots = 192. A few more CC chips are needed on the Roman Pot station card to reduce the number of bits further to less than 20 per Roman Pot station.
2. It is controlled by means of I2C and as such is fully integrated with the TOTEM standard control system.
3. It offers very minimal latency (less than a clock cycle) and is therefore ideally suited to match the severe trigger latency requirements for the Roman Pot system to be compatible with the CMS global trigger timing.
4. It provides a feature to extract count rates very useful for system debugging.

8 Annex 1: full list of pads

The following table contains a detailed list of pads.

PAD	FUNCTION					PAD	FUNCTION				
		lvds		X	Y			lvds		X	Y
1	IN	25	-	329,28	4305	73	IN	57	-	755	329,28
2	IN	25	+	114,28	4255	74	IN	57	+	705	114,28
3	IN	26	-	329,28	4205	75	IN	58	-	855	329,28
4	IN	26	+	114,28	4155	76	IN	58	+	805	114,28
5	IN	27	-	329,28	4105	77	IN	59	-	955	329,28
6	IN	27	+	114,28	4055	78	IN	59	+	905	114,28
7	IN	28	-	329,28	4005	79	IN	60	-	1055	329,28
8	IN	28	+	114,28	3955	80	IN	60	+	1005	114,28
9	IN	29	-	329,28	3905	81	IN	61	-	1155	329,28
10	IN	29	+	114,28	3855	82	IN	61	+	1105	114,28
11	IN	30	-	329,28	3805	83	IN	62	-	1255	329,28
12	IN	30	+	114,28	3755	84	IN	62	+	1205	114,28
13	IN	31	-	329,28	3705	85	IN	63	-	1355	329,28
14	IN	31	+	114,28	3655	86	IN	63	+	1305	114,28
15	IN	32	-	329,28	3605	87	IN	64	-	1455	329,28
16	IN	32	+	114,28	3555	88	IN	64	+	1405	114,28
17	VDD	in		329,28	3505	89	VDD	in		1555	329,28
18	GND	in		114,28	3455	90	GND	in		1505	114,28
19	VDD	in		329,28	3405	91	VDD	in		1655	329,28
20	GND	in		114,28	3355	92	GND	in		1605	114,28
21	IN	33	-	329,28	3305	93	IN	65	-	1755	329,28
22	IN	33	+	114,28	3255	94	IN	65	+	1705	114,28
23	IN	34	-	329,28	3205	95	IN	66	-	1855	329,28
24	IN	34	+	114,28	3155	96	IN	66	+	1805	114,28
25	IN	35	-	329,28	3105	97	IN	67	-	1955	329,28
26	IN	35	+	114,28	3055	98	IN	67	+	1905	114,28
27	IN	36	-	329,28	3005	99	IN	68	-	2055	329,28
28	IN	36	+	114,28	2955	100	IN	68	+	2005	114,28
29	IN	37	-	329,28	2905	101	IN	69	-	2155	329,28
30	IN	37	+	114,28	2855	102	IN	69	+	2105	114,28
31	IN	38	-	329,28	2805	103	IN	70	-	2255	329,28
32	IN	38	+	114,28	2755	104	IN	70	+	2205	114,28
33	IN	39	-	329,28	2705	105	IN	71	-	2355	329,28
34	IN	39	+	114,28	2655	106	IN	71	+	2305	114,28
35	IN	40	-	329,28	2605	107	IN	72	-	2455	329,28
36	IN	40	+	114,28	2555	108	IN	72	+	2405	114,28
37	IN	41	-	329,28	2505	109	IN	73	-	2555	329,28
38	IN	41	+	114,28	2455	110	IN	73	+	2505	114,28
39	IN	42	-	329,28	2405	111	IN	74	-	2655	329,28
40	IN	42	+	114,28	2355	112	IN	74	+	2605	114,28
41	IN	43	-	329,28	2305	113	IN	75	-	2755	329,28
42	IN	43	+	114,28	2255	114	IN	75	+	2705	114,28

43	IN	44	-	329,28	2205	115	IN	76	-	2855	329,28
44	IN	44	+	114,28	2155	116	IN	76	+	2805	114,28
45	IN	45	-	329,28	2105	117	IN	77	-	2955	329,28
46	IN	45	+	114,28	2055	118	IN	77	+	2905	114,28
47	IN	46	-	329,28	2005	119	IN	78	-	3055	329,28
48	IN	46	+	114,28	1955	120	IN	78	+	3005	114,28
49	IN	47	-	329,28	1905	121	IN	79	-	3155	329,28
50	IN	47	+	114,28	1855	122	IN	79	+	3105	114,28
51	IN	48	-	329,28	1805	123	IN	80	-	3255	329,28
52	IN	48	+	114,28	1755	124	IN	80	+	3205	114,28
53	VDD	in		329,28	1705	125	VDD	in		3355	329,28
54	GND	in		114,28	1655	126	GND	in		3305	114,28
55	VDD	in		329,28	1605	127	VDD	in		3455	329,28
56	GND	in		114,28	1555	128	GND	in		3405	114,28
57	IN	49	-	329,28	1505	129	CLKOUT			3705	329,28
58	IN	49	+	114,28	1455	130	CLKIN			3605	114,28
59	IN	50	-	329,28	1405	131	CLKlvdsin-			3905	329,28
60	IN	50	+	114,28	1355	132	GND			3805	114,28
61	IN	51	-	329,28	1305	133	CLKlvdsout+			4105	329,28
62	IN	51	+	114,28	1255	134	CLKlvdsin+			4005	114,28
63	IN	52	-	329,28	1205	135	VDD			4305	329,28
64	IN	52	+	114,28	1155	136	CLKlvdsout-	clock		4205	114,28
65	IN	53	-	329,28	1105						
66	IN	53	+	114,28	1055						
67	IN	54	-	329,28	1005						
68	IN	54	+	114,28	955						
69	IN	55	-	329,28	905						
70	IN	55	+	114,28	855						
71	IN	56	-	329,28	805						
72	IN	56	+	114,28	755						

PAD	FUNCTION			X	Y	PAD	FUNCTION			X	Y
137	OUT	16	+	4693,22	867,5	173	ForceREhBOff			4205	4700,72
138	GND			4908,22	767,5	174	REhB		I2C	4305	4915,72
139	OUT	15	+	4693,22	1067,5	175	VDD		I2C	4005	4700,72
140	OUT	16	-	4908,22	967,5	176	GND		I2C	4105	4915,72
141	OUT	14	+	4693,22	1267,5	177	SDA		I2C	3805	4700,72
142	OUT	15	-	4908,22	1167,5	178	REsB		I2C	3905	4915,72
143	OUT	13	+	4693,22	1467,5	179	ChipAdd<4>		I2C	3605	4700,72
144	OUT	14	-	4908,22	1367,5	180	SCL			3705	4915,72
145	OUT	12	+	4693,22	1667,5	181	ChipAdd<6>			3405	4700,72
146	OUT	13	-	4908,22	1567,5	182	ChipAdd<5>			3505	4915,72
147	OUT	11	+	4693,22	1867,5						
148	OUT	12	-	4908,22	1767,5		lvds				
149	OUT	10	+	4693,22	2067,5	183	IN	1	-	3205	4700,72
150	OUT	11	-	4908,22	1967,5	184	IN	1	+	3255	4915,72

151	OUT	9	+	4693,22	2267,5	185	IN	2	-	3105	4700,72
152	OUT	10	-	4908,22	2167,5	186	IN	2	+	3155	4915,72
153	VDD			4693,22	2467,5	187	IN	3	-	3005	4700,72
154	OUT	9	-	4908,22	2367,5	188	IN	3	+	3055	4915,72
155	OUT	8	+	4693,22	2667,5	189	IN	4	-	2905	4700,72
156	VDD			4908,22	2567,5	190	IN	4	+	2955	4915,72
157	OUT	7	+	4693,22	2867,5	191	IN	5	-	2805	4700,72
158	OUT	8	-	4908,22	2767,5	192	IN	5	+	2855	4915,72
159	OUT	6	+	4693,22	3067,5	193	IN	6	-	2705	4700,72
160	OUT	7	-	4908,22	2967,5	194	IN	6	+	2755	4915,72
161	OUT	5	+	4693,22	3267,5	195	IN	7	-	2605	4700,72
162	OUT	6	-	4908,22	3167,5	196	IN	7	+	2655	4915,72
163	OUT	4	+	4693,22	3467,5	197	IN	8	-	2505	4700,72
164	OUT	5	-	4908,22	3367,5	198	IN	8	+	2555	4915,72
165	OUT	3	+	4693,22	3667,5	199	IN	9	-	2405	4700,72
166	OUT	4	-	4908,22	3567,5	200	IN	9	+	2455	4915,72
167	OUT	2	+	4693,22	3867,5	201	IN	10	-	2305	4700,72
168	OUT	3	-	4908,22	3767,5	202	IN	10	+	2355	4915,72
169	OUT	1	+	4693,22	4067,5	203	IN	11	-	2205	4700,72
170	OUT	2	-	4908,22	3967,5	204	IN	11	+	2255	4915,72
171	GND			4693,22	4267,5	205	IN	12	-	2105	4700,72
172	OUT	1	-	4908,22	4167,5	206	IN	12	+	2155	4915,72
						207	IN	13	-	2005	4700,72
						208	IN	13	+	2055	4915,72
						209	IN	14	-	1905	4700,72
						210	IN	14	+	1955	4915,72
						211	IN	15	-	1805	4700,72
						212	IN	15	+	1855	4915,72
						213	IN	16	-	1705	4700,72
						214	IN	16	+	1755	4915,72
						215	VDD			1605	4700,72
						216	GND			1655	4915,72
						217	VDD			1505	4700,72
						218	GND			1555	4915,72
						219	IN	17	-	1405	4700,72
						220	IN	17	+	1455	4915,72
						221	IN	18	-	1305	4700,72
						222	IN	18	+	1355	4915,72
						223	IN	19	-	1205	4700,72
						224	IN	19	+	1255	4915,72
						225	IN	20	-	1105	4700,72
						226	IN	20	+	1155	4915,72
						227	IN	21	-	1005	4700,72
						228	IN	21	+	1055	4915,72
						229	IN	22	-	905	4700,72
						230	IN	22	+	955	4915,72

						231	IN	23	-	805	4700,72
						232	IN	23	+	855	4915,72
						233	IN	24	-	705	4700,72
						234	IN	24	+	755	4915,72

9 Annexe 2: CC-TEST

TEST1 (test de la synchronisation + Vout of NP + la totalité des entrees/sorties avec le test 2)							TEST2 (test de la polarité + entrees/sorties)						
Entree		valeur	Mask	sortie		valeur	Entree		valeur	Mask	sortie		valeur
IN	1	1	0	OUT	1	0	IN	1	1	0	OUT	1	1
IN	2	1	0	OUT	2	0	IN	2	1	0	OUT	2	1
IN	3	0	0	OUT	3	1	IN	3	0	0	OUT	3	0
IN	4	0	0	OUT	4	1	IN	4	0	0	OUT	4	0
IN	5	1	0	OUT	5	0	IN	5	1	0	OUT	5	1
IN	6	1	0	OUT	6	0	IN	6	1	0	OUT	6	1
IN	7	0	0	OUT	7	1	IN	7	0	0	OUT	7	0
IN	8	0	0	OUT	8	1	IN	8	0	0	OUT	8	0
IN	9	1	0	OUT	9	0	IN	9	1	0	OUT	9	1
IN	10	1	0	OUT	10	0	IN	10	1	0	OUT	10	1
IN	11	0	0	OUT	11	1	IN	11	0	0	OUT	11	0
IN	12	0	0	OUT	12	1	IN	12	0	0	OUT	12	0
IN	13	1	0	OUT	13	0	IN	13	1	0	OUT	13	1
IN	14	1	0	OUT	14	0	IN	14	1	0	OUT	14	1
IN	15	0	0	OUT	15	1	IN	15	0	0	OUT	15	0
IN	16	0	0	OUT	16	1	IN	16	0	0	OUT	16	0
IN	17	1	0				IN	17	1	0			
IN	18	1	0				IN	18	1	0			
IN	19	0	0				IN	19	0	0			
IN	20	0	0				IN	20	0	0			
IN	21	1	0				IN	21	1	0			
IN	22	1	0				IN	22	1	0			
IN	23	0	0				IN	23	0	0			
IN	24	0	0				IN	24	0	0			
IN	25	1	0				IN	25	1	0			
IN	26	1	0				IN	26	1	0			
IN	27	0	0				IN	27	0	0			
IN	28	0	0				IN	28	0	0			
IN	29	1	0				IN	29	1	0			
IN	30	1	0				IN	30	1	0			
IN	31	0	0				IN	31	0	0			
IN	32	0	0				IN	32	0	0			
IN	33	1	0				IN	33	1	0			
IN	34	1	0				IN	34	1	0			
IN	35	0	0				IN	35	0	0			
IN	36	0	0				IN	36	0	0			
IN	37	1	0				IN	37	1	0			
IN	38	1	0				IN	38	1	0			
IN	39	0	0				IN	39	0	0			
IN	40	0	0				IN	40	0	0			

IN	41	1	0				IN	41	1	0				
IN	42	1	0				IN	42	1	0				
IN	43	0	0				IN	43	0	0				
IN	44	0	0				IN	44	0	0				
IN	45	1	0				IN	45	1	0				
IN	46	1	0				IN	46	1	0				
IN	47	0	0				IN	47	0	0				
IN	48	0	0				IN	48	0	0				
IN	49	1	0				IN	49	1	0				
IN	50	1	0				IN	50	1	0				
IN	51	0	0				IN	51	0	0				
IN	52	0	0				IN	52	0	0				
IN	53	1	0				IN	53	1	0				
IN	54	1	0				IN	54	1	0				
IN	55	0	0				IN	55	0	0				
IN	56	0	0				IN	56	0	0				
IN	57	1	0				IN	57	1	0				
IN	58	1	0				IN	58	1	0				
IN	59	0	0				IN	59	0	0				
IN	60	0	0				IN	60	0	0				
IN	61	1	0				IN	61	1	0				
IN	62	1	0				IN	62	1	0				
IN	63	0	0				IN	63	0	0				
IN	64	0	0				IN	64	0	0				
IN	65	1	0				IN	65	1	0				
IN	66	1	0				IN	66	1	0				
IN	67	0	0				IN	67	0	0				
IN	68	0	0				IN	68	0	0				
IN	69	1	0				IN	69	1	0				
IN	70	1	0				IN	70	1	0				
IN	71	0	0				IN	71	0	0				
IN	72	0	0				IN	72	0	0				
IN	73	1	0				IN	73	1	0				
IN	74	1	0				IN	74	1	0				
IN	75	0	0				IN	75	0	0				
IN	76	0	0				IN	76	0	0				
IN	77	1	0				IN	77	1	0				
IN	78	1	0				IN	78	1	0				
IN	79	0	0				IN	79	0	0				
IN	80	0	0				IN	80	0	0				

TEST3 (test W out of NP + And/Or + stretcher)						
Entree		valeur	Mask	sortie		valeur
IN	1	0	0	OUT	1	0
IN	2	0	0	OUT	2	0
IN	3	0	0	OUT	3	1
IN	4	1	0	OUT	4	1
IN	5	0	0	OUT	5	1
IN	6	0	0	OUT	6	1
IN	7	1	0	OUT	7	1
IN	8	1	0	OUT	8	1
IN	9	0	0	OUT	9	1
IN	10	0	0	OUT	10	0

TEST4 (test W out of NP et NP)						
Entree		valeur	Mask	sortie		valeur
IN	1	0	0	OUT	1	0
IN	2	0	0	OUT	2	0
IN	3	0	0	OUT	3	1
IN	4	1	0	OUT	4	1
IN	5	0	0	OUT	5	1
IN	6	0	0	OUT	6	0
IN	7	1	0	OUT	7	1
IN	8	1	0	OUT	8	1
IN	9	0	0	OUT	9	0
IN	10	0	0	OUT	10	0

IN	11	0	0	OUT	11	1	IN	11	0	0	OUT	11	1
IN	12	1	0	OUT	12	1	IN	12	1	0	OUT	12	1
IN	13	0	0	OUT	13	1	IN	13	0	0	OUT	13	1
IN	14	0	0	OUT	14	0	IN	14	0	0	OUT	14	0
IN	15	0	0	OUT	15	1	IN	15	0	0	OUT	15	1
IN	16	1	0	OUT	16	1	IN	16	1	0	OUT	16	1
IN	17	0	0				IN	17	0	0			
IN	18	0	0				IN	18	0	0			
IN	19	0	0				IN	19	0	0			
IN	20	1	0				IN	20	1	0			
IN	21	0	0				IN	21	0	0			
IN	22	0	0				IN	22	0	0			
IN	23	1	0				IN	23	1	0			
IN	24	1	0				IN	24	1	0			
IN	25	0	0				IN	25	0	0			
IN	26	0	0				IN	26	0	0			
IN	27	0	0				IN	27	0	0			
IN	28	1	0				IN	28	1	0			
IN	29	0	0				IN	29	0	0			
IN	30	0	0				IN	30	0	0			
IN	31	0	0				IN	31	0	0			
IN	32	1	0				IN	32	1	0			
IN	33	0	0				IN	33	0	0			
IN	34	0	0				IN	34	0	0			
IN	35	0	0				IN	35	0	0			
IN	36	1	0				IN	36	1	0			
IN	37	0	0				IN	37	0	0			
IN	38	0	0				IN	38	0	0			
IN	39	1	0				IN	39	1	0			
IN	40	1	0				IN	40	1	0			
IN	41	0	0				IN	41	0	0			
IN	42	0	0				IN	42	0	0			
IN	43	0	0				IN	43	0	0			
IN	44	1	0				IN	44	1	0			
IN	45	0	0				IN	45	0	0			
IN	46	0	0				IN	46	0	0			
IN	47	0	0				IN	47	0	0			
IN	48	1	0				IN	48	1	0			
IN	49	0	0				IN	49	0	0			
IN	50	0	0				IN	50	0	0			
IN	51	0	0				IN	51	0	0			
IN	52	1	0				IN	52	1	0			
IN	53	0	0				IN	53	0	0			
IN	54	0	0				IN	54	0	0			
IN	55	1	0				IN	55	1	0			
IN	56	1	0				IN	56	1	0			
IN	57	0	0				IN	57	0	0			
IN	58	0	0				IN	58	0	0			
IN	59	0	0				IN	59	0	0			
IN	60	1	0				IN	60	1	0			
IN	61	0	0				IN	61	0	0			
IN	62	0	0				IN	62	0	0			
IN	63	0	0				IN	63	0	0			

IN	64	1	0			
IN	65	0	0			
IN	66	0	0			
IN	67	0	0			
IN	68	1	0			
IN	69	0	0			
IN	70	0	0			
IN	71	1	0			
IN	72	1	0			
IN	73	0	0			
IN	74	0	0			
IN	75	0	0			
IN	76	1	0			
IN	77	0	0			
IN	78	0	0			
IN	79	0	0			
IN	80	1	0			

TEST5 (test de And/Or + front des sorties)

Entree		valeur	Mask	sortie		valeur
IN	1	0	0	OUT	1	0
IN	2	0	0	OUT	2	0
IN	3	1	0	OUT	3	1
IN	4	1	0	OUT	4	1
IN	5	0	0	OUT	5	0
IN	6	0	0	OUT	6	0
IN	7	1	0	OUT	7	1
IN	8	1	0	OUT	8	1
IN	9	0	0	OUT	9	0
IN	10	0	0	OUT	10	0
IN	11	1	0	OUT	11	1
IN	12	1	0	OUT	12	1
IN	13	0	0	OUT	13	0
IN	14	0	0	OUT	14	0
IN	15	1	0	OUT	15	1
IN	16	1	0	OUT	16	1
IN	17	0	0			
IN	18	0	0			
IN	19	1	0			
IN	20	1	0			
IN	21	0	0			
IN	22	0	0			
IN	23	1	0			
IN	24	1	0			
IN	25	0	0			
IN	26	0	0			
IN	27	1	0			
IN	28	1	0			
IN	29	0	0			
IN	30	0	0			
IN	31	1	0			
IN	32	1	0			
IN	33	0	0			

IN	64	1	0			
IN	65	0	0			
IN	66	0	0			
IN	67	0	0			
IN	68	1	0			
IN	69	0	0			
IN	70	0	0			
IN	71	1	0			
IN	72	1	0			
IN	73	0	0			
IN	74	0	0			
IN	75	0	0			
IN	76	1	0			
IN	77	0	0			
IN	78	0	0			
IN	79	0	0			
IN	80	1	0			

TEST6 (test Z out of 16)

Entree		valeur	Mask	sortie		valeur
IN	1	0	0	OUT	1	0
IN	2	0	0	OUT	2	0
IN	3	1	0	OUT	3	0
IN	4	1	0	OUT	4	0
IN	5	0	0	OUT	5	0
IN	6	0	0	OUT	6	0
IN	7	1	0	OUT	7	0
IN	8	1	0	OUT	8	0
IN	9	0	0	OUT	9	0
IN	10	0	0	OUT	10	0
IN	11	1	0	OUT	11	0
IN	12	1	0	OUT	12	0
IN	13	0	0	OUT	13	0
IN	14	0	0	OUT	14	0
IN	15	1	0	OUT	15	0
IN	16	1	0	OUT	16	0
IN	17	0	0			
IN	18	0	0			
IN	19	1	0			
IN	20	1	0			
IN	21	0	0			
IN	22	0	0			
IN	23	1	0			
IN	24	1	0			
IN	25	0	0			
IN	26	0	0			
IN	27	1	0			
IN	28	1	0			
IN	29	0	0			
IN	30	0	0			
IN	31	1	0			
IN	32	1	0			
IN	33	0	0			

IN	34	0	0				IN	34	0	0			
IN	35	1	0				IN	35	1	0			
IN	36	1	0				IN	36	1	0			
IN	37	0	0				IN	37	0	0			
IN	38	0	0				IN	38	0	0			
IN	39	1	0				IN	39	1	0			
IN	40	1	0				IN	40	1	0			
IN	41	0	0				IN	41	0	0			
IN	42	0	0				IN	42	0	0			
IN	43	1	0				IN	43	1	0			
IN	44	1	0				IN	44	1	0			
IN	45	0	0				IN	45	0	0			
IN	46	0	0				IN	46	0	0			
IN	47	1	0				IN	47	1	0			
IN	48	1	0				IN	48	1	0			
IN	49	0	0				IN	49	0	0			
IN	50	0	0				IN	50	0	0			
IN	51	1	0				IN	51	1	0			
IN	52	1	0				IN	52	1	0			
IN	53	0	0				IN	53	0	0			
IN	54	0	0				IN	54	0	0			
IN	55	1	0				IN	55	1	0			
IN	56	1	0				IN	56	1	0			
IN	57	0	0				IN	57	0	0			
IN	58	0	0				IN	58	0	0			
IN	59	1	0				IN	59	1	0			
IN	60	1	0				IN	60	1	0			
IN	61	0	0				IN	61	0	0			
IN	62	0	0				IN	62	0	0			
IN	63	1	0				IN	63	1	0			
IN	64	1	0				IN	64	1	0			
IN	65	0	0				IN	65	0	0			
IN	66	0	0				IN	66	0	0			
IN	67	1	0				IN	67	1	0			
IN	68	1	0				IN	68	1	0			
IN	69	0	0				IN	69	0	0			
IN	70	0	0				IN	70	0	0			
IN	71	1	0				IN	71	1	0			
IN	72	1	0				IN	72	1	0			
IN	73	0	0				IN	73	0	0			
IN	74	0	0				IN	74	0	0			
IN	75	1	0				IN	75	1	0			
IN	76	1	0				IN	76	1	0			
IN	77	0	0				IN	77	0	0			
IN	78	0	0				IN	78	0	0			
IN	79	1	0				IN	79	1	0			
IN	80	1	0				IN	80	1	0			

TEST7(test du mask)						
Entree		valeur	Mask	sortie		valeur
IN	1	0	1	OUT	1	0
IN	2	0	1	OUT	2	0
IN	3	1	1	OUT	3	0

TEST8 (Zout of 16 + And/Or2 + O2)						
Entree		valeur	Mask	sortie		valeur
IN	1	0	1	OUT	1	0
IN	2	0	1	OUT	2	0
IN	3	1	1	OUT	3	0

IN	4	1	1	OUT	4	0	IN	4	1	1	OUT	4	0
IN	5	0	1	OUT	5	0	IN	5	0	1	OUT	5	0
IN	6	0	1	OUT	6	0	IN	6	0	1	OUT	6	0
IN	7	1	1	OUT	7	0	IN	7	1	1	OUT	7	0
IN	8	1	1	OUT	8	0	IN	8	1	1	OUT	8	0
IN	9	0	1	OUT	9	0	IN	9	0	1	OUT	9	0
IN	10	0	1	OUT	10	0	IN	10	0	1	OUT	10	0
IN	11	1	1	OUT	11	0	IN	11	1	1	OUT	11	0
IN	12	1	1	OUT	12	0	IN	12	1	1	OUT	12	0
IN	13	0	1	OUT	13	0	IN	13	0	1	OUT	13	0
IN	14	0	1	OUT	14	0	IN	14	0	1	OUT	14	0
IN	15	1	1	OUT	15	0	IN	15	1	1	OUT	15	1
IN	16	1	1	OUT	16	0	IN	16	1	1	OUT	16	0
IN	17	0	1				IN	17	0	1			
IN	18	0	1				IN	18	0	1			
IN	19	1	1				IN	19	1	1			
IN	20	1	1				IN	20	1	1			
IN	21	0	1				IN	21	0	1			
IN	22	0	1				IN	22	0	1			
IN	23	1	1				IN	23	1	1			
IN	24	1	1				IN	24	1	1			
IN	25	0	1				IN	25	0	1			
IN	26	0	1				IN	26	0	1			
IN	27	1	1				IN	27	1	1			
IN	28	1	1				IN	28	1	1			
IN	29	0	1				IN	29	0	1			
IN	30	0	1				IN	30	0	1			
IN	31	1	1				IN	31	1	1			
IN	32	1	1				IN	32	1	1			
IN	33	0	1				IN	33	0	1			
IN	34	0	1				IN	34	0	1			
IN	35	1	1				IN	35	1	1			
IN	36	1	1				IN	36	1	1			
IN	37	0	1				IN	37	0	1			
IN	38	0	1				IN	38	0	1			
IN	39	1	1				IN	39	1	1			
IN	40	1	1				IN	40	1	1			
IN	41	0	1				IN	41	0	0			
IN	42	0	1				IN	42	0	0			
IN	43	1	1				IN	43	1	0			
IN	44	1	1				IN	44	1	0			
IN	45	0	1				IN	45	0	0			
IN	46	0	1				IN	46	0	0			
IN	47	1	1				IN	47	1	0			
IN	48	1	1				IN	48	1	0			
IN	49	0	1				IN	49	0	0			
IN	50	0	1				IN	50	0	0			
IN	51	1	1				IN	51	1	0			
IN	52	1	1				IN	52	1	0			
IN	53	0	1				IN	53	0	0			
IN	54	0	1				IN	54	0	0			
IN	55	1	1				IN	55	1	0			
IN	56	1	1				IN	56	1	0			

IN	57	0	1				IN	57	0	0			
IN	58	0	1				IN	58	0	0			
IN	59	1	1				IN	59	1	0			
IN	60	1	1				IN	60	1	0			
IN	61	0	1				IN	61	0	0			
IN	62	0	1				IN	62	0	0			
IN	63	1	1				IN	63	1	0			
IN	64	1	1				IN	64	1	0			
IN	65	0	1				IN	65	0	0			
IN	66	0	1				IN	66	0	0			
IN	67	1	1				IN	67	1	0			
IN	68	1	1				IN	68	1	0			
IN	69	0	1				IN	69	0	0			
IN	70	0	1				IN	70	0	0			
IN	71	1	1				IN	71	1	0			
IN	72	1	1				IN	72	1	0			
IN	73	0	1				IN	73	0	0			
IN	74	0	1				IN	74	0	0			
IN	75	1	1				IN	75	1	0			
IN	76	1	1				IN	76	1	0			
IN	77	0	1				IN	77	0	0			
IN	78	0	1				IN	78	0	0			
IN	79	1	1				IN	79	1	0			
IN	80	1	1				IN	80	1	0			

Organisation of the coincidence I2C registers for the different tests:

TEST1

Control Register 0							
7	6	5	4	3	2	1	O
-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S
		0	0		0	1	1
Control Register 1							
7	6	5	4	3	2	1	O
OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)
0	0	0	1	0	0	1	1
Control Register 2							
7	6	5	4	3	2	1	O
Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)
1	1	1	1	0	0	0	0
Control Register 3							
7	6	5	4	3	2	1	O
AO(1)	AO(0	LO(1)	LO(0)	LI	O2(2)	O2(1)	O2(0)
1	0	0	0	0	0	0	0
Control Register 4							
7	6	5	4	3	2	1	O
CL	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)
0	0	0	1	0	0	0	0
Control Register 10							
Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)
0	0	0	0	0	0	0	0
Control Register 11							
7	6	5	4	3	2	1	O
Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask11)	Mask(10)	Mask(9)	Mask(8)
0	0	0	0	0	0	0	0
Control Register 12							
7	6	5	4	3	2	1	O
Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)
0	0	0	0	0	0	0	0
Control Register 10							
7	6	5	4	3	2	1	O
Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)
0	0	0	0	0	0	0	0

Control Register 13							
7	6	5	4	3	2	1	O
Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)
0	0	0	0	0	0	0	0
Control Register 0 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)
0	0	0	0	0	0	0	0
Control Register 1 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)
0	0	0	0	0	0	0	0
Control Register 2 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)
0	0	0	0	0	0	0	0
Control Register 3 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)
0	0	0	0	0	0	0	0
Control Register 4 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)
0	0	0	0	0	0	0	0

TEST2

Control Register 0							
7	6	5	4	3	2	1	O
-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S
		0	0		1	0	1
Control Register 1							
7	6	5	4	3	2	1	O
OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)
0	0	0	1	0	0	1	1
Control Register 2							
7	6	5	4	3	2	1	O
Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)
1	1	1	1	0	0	0	0

Control Register 3							
7	6	5	4	3	2	1	O
AO(1)	AO(0	LO(1)	LO(0)	LI	O2(2)	O2(1)	O2(0)
1	0	0	0	1	0	0	0
Control Register 4							
7	6	5	4	3	2	1	O
CL	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)
0	0	0	1	0	0	0	0
Control Register 10							
Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)
0	0	0	0	0	0	0	0
Control Register 11							
7	6	5	4	3	2	1	O
Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask11)	Mask(10)	Mask(9)	Mask(8)
0	0	0	0	0	0	0	0
Control Register 12							
7	6	5	4	3	2	1	O
Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)
0	0	0	0	0	0	0	0
Control Register 10							
7	6	5	4	3	2	1	O
Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)
0	0	0	0	0	0	0	0
Control Register 13							
7	6	5	4	3	2	1	O
Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)
0	0	0	0	0	0	0	0
Control Register 0 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)
0	0	0	0	0	0	0	0
Control Register 1 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)
0	0	0	0	0	0	0	0
Control Register 2 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)
0	0	0	0	0	0	0	0
Control Register 3 (EXTREG)							
7	6	5	4	3	2	1	O

Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)
0	0	0	0	0	0	0	0
Control Register 4 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)
0	0	0	0	0	0	0	0

TEST3

Control Register 0							
7	6	5	4	3	2	1	O
-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S
		0	0		0	1	1
Control Register 1							
7	6	5	4	3	2	1	O
OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)
0	0	1	1	0	0	1	1
Control Register 2							
7	6	5	4	3	2	1	O
Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)
1	1	1	1	0	0	1	1
Control Register 3							
7	6	5	4	3	2	1	O
AO(1)	AO(0	LO(1)	LO(0)	LI	O2(2)	O2(1)	O2(0)
1	1	0	0	0	0	0	0
Control Register 4							
7	6	5	4	3	2	1	O
CL	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)
0	0	0	1	0	0	0	0
Control Register 10							
Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)
0	0	0	0	0	0	0	0
Control Register 11							
7	6	5	4	3	2	1	O
Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask11)	Mask(10)	Mask(9)	Mask(8)
0	0	0	0	0	0	0	0
Control Register 12							
7	6	5	4	3	2	1	O
Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)
0	0	0	0	0	0	0	0

Control Register 10							
7	6	5	4	3	2	1	O
Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)
0	0	0	0	0	0	0	0
Control Register 13							
7	6	5	4	3	2	1	O
Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)
0	0	0	0	0	0	0	0
Control Register 0 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)
0	0	0	0	0	0	0	0
Control Register 1 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)
0	0	0	0	0	0	0	0
Control Register 2 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)
0	0	0	0	0	0	0	0
Control Register 3 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)
0	0	0	0	0	0	0	0
Control Register 4 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)
0	0	0	0	0	0	0	0

TEST4

Control Register 0							
7	6	5	4	3	2	1	O
-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S
		0	0		0	1	1
Control Register 1							
7	6	5	4	3	2	1	O
OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)
0	0	1	0	0	0	1	1

Control Register 2							
7	6	5	4	3	2	1	O
Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)
1	1	1	1	0	1	1	0
Control Register 3							
7	6	5	4	3	2	1	O
AO(1)	AO(0	LO(1)	LO(0)	LI	O2(2)	O2(1)	O2(0)
1	1	0	0	0	0	0	0
Control Register 4							
7	6	5	4	3	2	1	O
CL	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)
0	0	0	1	0	0	0	0
Control Register 10							
Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)
0	0	0	0	0	0	0	0
Control Register 11							
7	6	5	4	3	2	1	O
Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask11)	Mask(10)	Mask(9)	Mask(8)
0	0	0	0	0	0	0	0
Control Register 12							
7	6	5	4	3	2	1	O
Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)
0	0	0	0	0	0	0	0
Control Register 10							
7	6	5	4	3	2	1	O
Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)
0	0	0	0	0	0	0	0
Control Register 13							
7	6	5	4	3	2	1	O
Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)
0	0	0	0	0	0	0	0
Control Register 0 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)
0	0	0	0	0	0	0	0
Control Register 1 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)
0	0	0	0	0	0	0	0
Control Register 2 (EXTREG)							
7	6	5	4	3	2	1	O

Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)
0	0	0	0	0	0	0	0
Control Register 3 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)
0	0	0	0	0	0	0	0
Control Register 4 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)
0	0	0	0	0	0	0	0

TEST5

Control Register 0							
7	6	5	4	3	2	1	O
-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S
		0	0		0	1	1
Control Register 1							
7	6	5	4	3	2	1	O
OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)
0	1	0	1	0	0	1	1
Control Register 2							
7	6	5	4	3	2	1	O
Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)
1	1	1	1	0	0	1	1
Control Register 3							
7	6	5	4	3	2	1	O
AO(1)	AO(0	LO(1)	LO(0)	LI	O2(2)	O2(1)	O2(0)
0	0	0	0	0	0	0	0
Control Register 4							
7	6	5	4	3	2	1	O
CL	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)
1	0	1	1	0	0	0	0
Control Register 10							
Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)
0	0	0	0	0	0	0	0
Control Register 11							
7	6	5	4	3	2	1	O
Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask11)	Mask(10)	Mask(9)	Mask(8)
0	0	0	0	0	0	0	0

Control Register 12							
7	6	5	4	3	2	1	O
Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)
0	0	0	0	0	0	0	0
Control Register 10							
7	6	5	4	3	2	1	O
Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)
0	0	0	0	0	0	0	0
Control Register 13							
7	6	5	4	3	2	1	O
Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)
0	0	0	0	0	0	0	0
Control Register 0 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)
0	0	0	0	0	0	0	0
Control Register 1 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)
0	0	0	0	0	0	0	0
Control Register 2 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)
0	0	0	0	0	0	0	0
Control Register 3 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)
0	0	0	0	0	0	0	0
Control Register 4 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)
0	0	0	0	0	0	0	0

TEST6

Control Register 0							
7	6	5	4	3	2	1	O
-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S
		0	0		0	1	1

Control Register 1							
7	6	5	4	3	2	1	O
OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)
0	0	0	0	0	0	1	1
Control Register 2							
7	6	5	4	3	2	1	O
Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)
0	0	1	0	0	0	1	1
Control Register 3							
7	6	5	4	3	2	1	O
AO(1)	AO(0	LO(1)	LO(0)	LI	O2(2)	O2(1)	O2(0)
1	0	0	0	0	0	0	0
Control Register 4							
7	6	5	4	3	2	1	O
CL	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)
0	0	1	1	0	0	0	0
Control Register 10							
Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)
0	0	0	0	0	0	0	0
Control Register 11							
7	6	5	4	3	2	1	O
Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask11)	Mask(10)	Mask(9)	Mask(8)
0	0	0	0	0	0	0	0
Control Register 12							
7	6	5	4	3	2	1	O
Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)
0	0	0	0	0	0	0	0
Control Register 10							
7	6	5	4	3	2	1	O
Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)
0	0	0	0	0	0	0	0
Control Register 13							
7	6	5	4	3	2	1	O
Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)
0	0	0	0	0	0	0	0
Control Register 0 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)
0	0	0	0	0	0	0	0
Control Register 1 (EXTREG)							
7	6	5	4	3	2	1	O

Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)
0	0	0	0	0	0	0	0
Control Register 2 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)
0	0	0	0	0	0	0	0
Control Register 3 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)
0	0	0	0	0	0	0	0
Control Register 4 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)
0	0	0	0	0	0	0	0

TEST7

Control Register 0							
7	6	5	4	3	2	1	O
-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S
		0	0		0	1	1
Control Register 1							
7	6	5	4	3	2	1	O
OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)
0	0	0	0	0	0	1	1
Control Register 2							
7	6	5	4	3	2	1	O
Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)
1	1	1	1	0	0	1	1
Control Register 3							
7	6	5	4	3	2	1	O
AO(1)	AO(0	LO(1)	LO(0)	LI	O2(2)	O2(1)	O2(0)
1	0	0	0	0	0	0	0
Control Register 4							
7	6	5	4	3	2	1	O
CL	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)
0	0	1	1	0	0	0	0
Control Register 10							
Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)
1	1	1	1	1	1	1	1

Control Register 11							
7	6	5	4	3	2	1	O
Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask11)	Mask(10)	Mask(9)	Mask(8)
1	1	1	1	1	1	1	1
Control Register 12							
7	6	5	4	3	2	1	O
Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)
1	1	1	1	1	1	1	1
Control Register 10							
7	6	5	4	3	2	1	O
Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)
1	1	1	1	1	1	1	1
Control Register 13							
7	6	5	4	3	2	1	O
Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)
1	1	1	1	1	1	1	1
Control Register 0 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)
1	1	1	1	1	1	1	1
Control Register 1 (EXTREG)							
Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)
1	1	1	1	1	1	1	1
Control Register 2 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)
1	1	1	1	1	1	1	1
Control Register 3 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)
1	1	1	1	1	1	1	1
Control Register 4 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)
1	1	1	1	1	1	1	1

TEST8

Control Register 0							
7	6	5	4	3	2	1	O
-	-	CT(1)	CT(0)	-	Sync2(1)	Sync(0)	S
		0	0		0	1	1
Control Register 1							
7	6	5	4	3	2	1	O
OV(2)	OV(1)	OV(0)	NP	V(3)	V(2)	V(1)	V(0)
0	0	0	0	0	0	1	1
Control Register 2							
7	6	5	4	3	2	1	O
Z(3)	Z(2)	Z(1)	Z(0)	W(3)	W(2)	W(1)	W(0)
0	0	1	0	0	0	1	1
Control Register 3							
7	6	5	4	3	2	1	O
AO(1)	AO(0	LO(1)	LO(0)	LI	O2(2)	O2(1)	O2(0)
1	0	0	1	0	1	0	0
Control Register 4							
7	6	5	4	3	2	1	O
CL	T(2)	T(1)	T(0)	CO(3)	CO(2)	CO(1)	CO(0)
0	0	1	1	0	0	0	0
Control Register 10							
Mask(7)	Mask(6)	Mask(5)	Mask(4)	Mask(3)	Mask(2)	Mask(1)	Mask(0)
1	1	1	1	1	1	1	1
Control Register 11							
7	6	5	4	3	2	1	O
Mask(15)	Mask(14)	Mask(13)	Mask(12)	Mask11)	Mask(10)	Mask(9)	Mask(8)
1	1	1	1	1	1	1	1
Control Register 12							
7	6	5	4	3	2	1	O
Mask(23)	Mask(22)	Mask(21)	Mask(20)	Mask(19)	Mask(18)	Mask(17)	Mask(16)
1	1	1	1	1	1	1	1
Control Register 10							
7	6	5	4	3	2	1	O
Mask(31)	Mask(30)	Mask(29)	Mask(28)	Mask(27)	Mask(26)	Mask(25)	Mask(24)
1	1	1	1	1	1	1	1
Control Register 13							
7	6	5	4	3	2	1	O
Mask(39)	Mask(38)	Mask(37)	Mask(36)	Mask(35)	Mask(34)	Mask(33)	Mask(32)
1	1	1	1	1	1	1	1

Control Register 0 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(47)	Mask(46)	Mask(45)	Mask(44)	Mask(43)	Mask(42)	Mask(41)	Mask(40)
0	0	0	0	0	0	0	0
Control Register 1 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(55)	Mask(54)	Mask(53)	Mask(52)	Mask(51)	Mask(50)	Mask(49)	Mask(48)
0	0	0	0	0	0	0	0
Control Register 2 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(63)	Mask(62)	Mask(61)	Mask(60)	Mask(59)	Mask(58)	Mask(57)	Mask(56)
0	0	0	0	0	0	0	0
Control Register 3 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(71)	Mask(70)	Mask(69)	Mask(68)	Mask(67)	Mask(66)	Mask(65)	Mask(64)
0	0	0	0	0	0	0	0
Control Register 4 (EXTREG)							
7	6	5	4	3	2	1	O
Mask(79)	Mask(78)	Mask(77)	Mask(76)	Mask(75)	Mask(74)	Mask(73)	Mask(72)
0	0	0	0	0	0	0	0