TOTEM Roman Pot Motherboard RPMB

Specification

Version 4

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TOTEM Roman Pot Motherboard

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1. Introduction

The TOTEM experiment has three sub-detectors: Roman Pots (RP) with silicon strips, T1 detector with Cathode Strip Chambers (CSC) and T2 with Gas Electron Multiplier detectors (GEM). All detectors use the VFAT chip for tracking and trigger generation mounted on different hybrids. A Roman Pot hybrid contains four VFAT chips. The set of ten hybrids is built for every Roman Pot.

The RPMB is connecting to this set via flex connections and glued to the flange. This document will give a detailed specification of the design and functionality of the RPMB, and its components as a part of the front-end electronics in Roman Pot for TOTEM experiment.

2. Block Diagram

The block diagram of the board with its connectivity to the hybrids is shown on Figure 1:

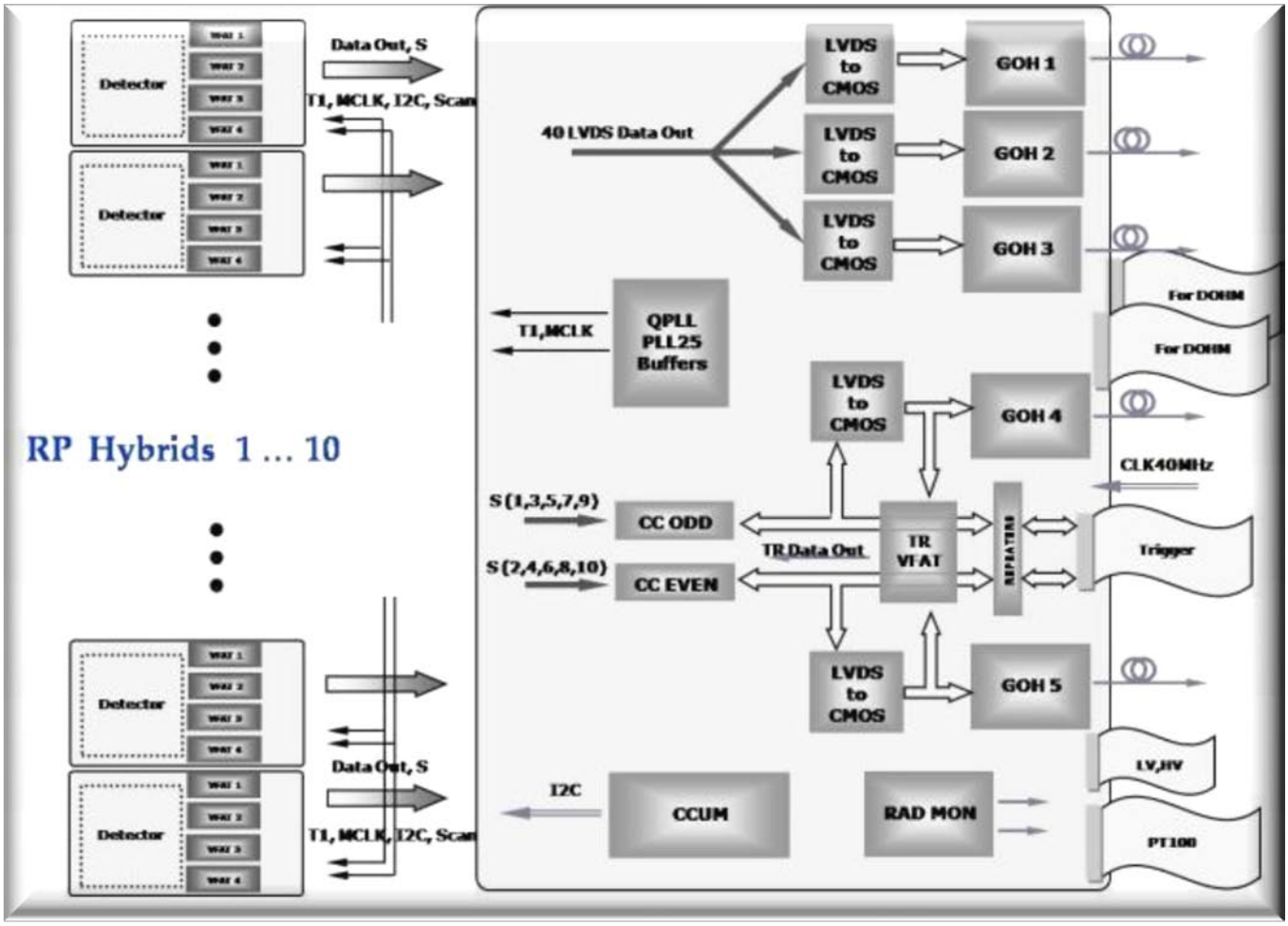

Figure 1 RPMB Block Diagram

3. Components

The design of the board is done so as to mount it on top of the Roman Pot. From one side it is connected to the RP Hybrids and from the other via the front panel to the counting room.
The board accepts several numbers of mezzanines card which will be described later in this document. A front panel with connectors for low and high voltage, control, data and trigger bits transfer is used to facilitate the connection to the central patch panel of the RP stations.

The "RPMB" contains the following general building blocks:

- *Control Logic Block* – based on CERN commonly used Communication and Control Unit CCUM mezzanine. This module is connected to the control loop (DOHM and FEC-CCS) via two 20pins 3M high speed connectors placed on the front panel. Control logic block provides 16 I^2C interface channels and one 8 bit parallel control port;
- *Clock and Commands Distribution Block* – based on PLL25 chip, QPLL and a number of clock and commands distribution circuitry to deliver synchronous clock and commands to every component on the board including the VFAT chips on the RP Hybrids;
- *Data Conversion and Transmission Block* – based on LVDS to CMOS converters and gigabit optical hybrids GOH modules. Three GOH modules are used to send data from 40 VTAF chips to the counting room;
- *Trigger Transmission Block* – based on Coincidence chip mezzanine, LVDS to CMOS converters, Trigger VFAT mezzanine and two GOH modules. To transmit trigger bits to the counting room two ways have been selected: optical fibers are used for the 150m RP station and in TOTEM standalone runs also for the 220m station. The runs with CMS on the other hand are subject to CMS's limited trigger latency time, imposing trigger bit transmission with LVDS signals through fast electrical cables. The electrical transmission over such a long distance requires care to preserve signal integrity. This can only be achieved by restoring the LVDS signals to full levels at regular intervals over the transmission distance. A special integrated circuit was designed for this purpose: the LVDS repeater chip can treat 16 LVDS channels in parallel and was designed according to a special layout to guarantee radiation tolerance. This chip will be mounted on a small repeater board. At regular intervals of about 70m a repeater station is introduced which consists of several repeater boards with cable connectors;
- *Slow Control Block* – includes digital/analog LV and HV power distribution, temperature, pressure and radiation monitoring. For measuring the temperature on the hybrids and inside in the pot the PT100/1000 sensors are being used. Special RADMON small mezzanine card is being used for radiation monitoring on the board.

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The RPMB is a 16-layers double-side printed circuits board from halogen-free material. The location in the experiment means that board will be exposed to different levels of radiation. That is why components on the board are specially designed by CERN microelectronics group using radiation hardness technology. Photo of the board top and bottom side without mezzanines is shown on Figure 2:

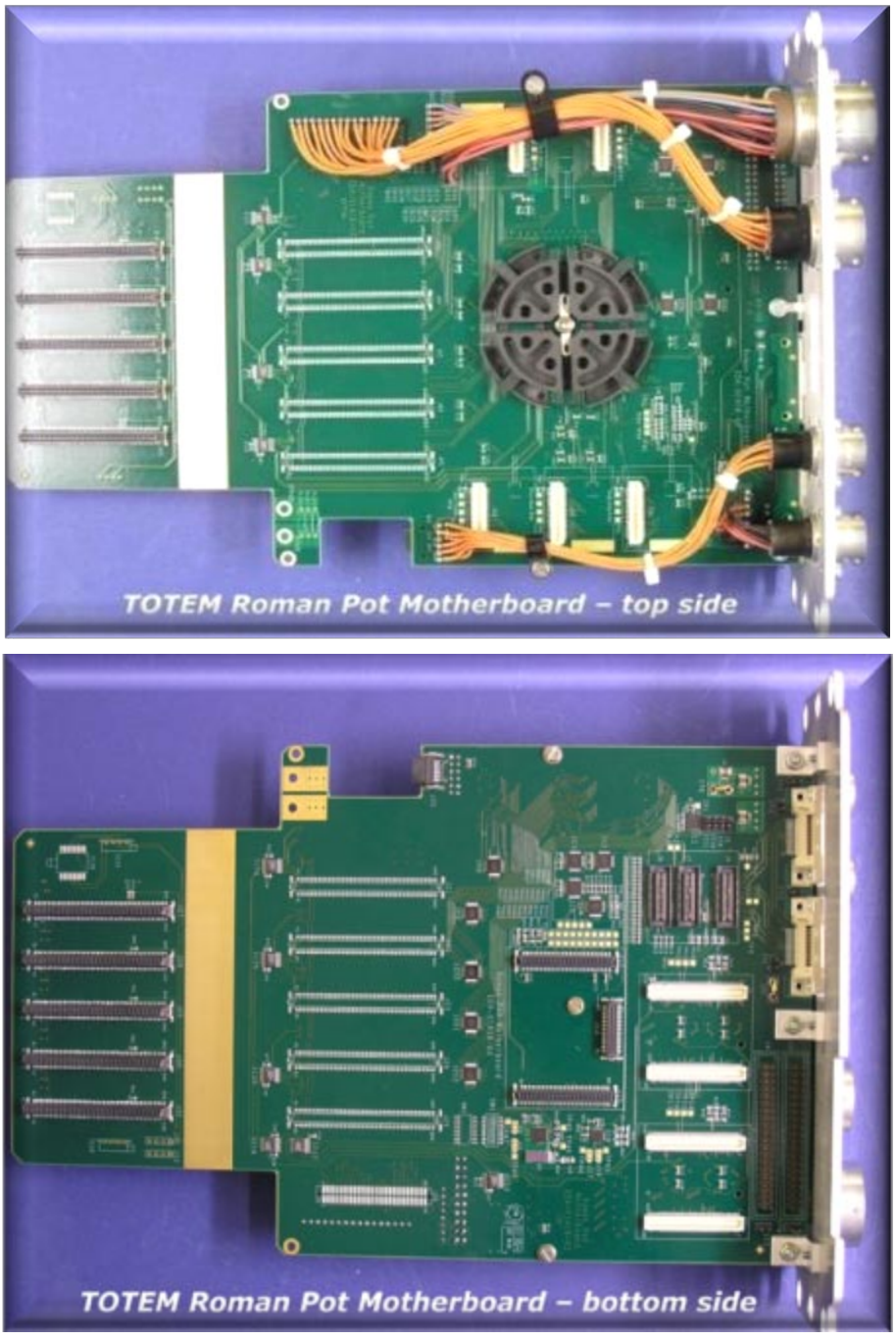

Figure 2 RPMB Photo – Top and Bottom side

3.1. Mezzanine Cards

On the motherboard the following mezzanines are implemented: Trigger VFAT, Coincidence Chip, CCUM, GOH and RADMON.

3.1.1. Trigger VFAT Mezzanine

Trigger VFAT mezzanine is being used to generate control signal from its BC0 test output and to serialize trigger bits from the VFAT's and send them via GOH optically to the counting room. The BC0 test output is meant to synchronize trigger bits on trigger GOH's. This synchronization is done by disabling the GOH's data valid signal for duration of one clock cycle. The photo of the mezzanine is shown on Figure 3.

Figure 3 Trigger VFAT mezzanine

3.1.2. Coincidence Chip Mezzanine

The VFAT's are generating fast signals which are used to provide the trigger signals provided by TOTEM to the CMS global trigger box. A full custom chip rather than using a Field Programmable Gate Array was developed for two main reasons:

1. The latency constraints on the generation of the trigger bits especially from the Roman Pots are very severe: after subtraction of cable delays only about 8-10 bunch crossings are left for the generation of the trigger signals to be provided to CMS from the signals generated by the Roman Pot detector front end. A full custom chip with dedicated logic can implement the required coincidence in one clock.
2. Special design techniques can make a full custom chip much more robust against radiation both with regard to the total dose and single event effects. This allows placing this chip in aggressive radiation environments, i.e. very close to the detectors.

Figure 4 CC Mezzanine

The special mezzanine was designed with one Coincidence Chip and two 130pins input/output connectors.

3.1.3. Slow Control and CCUM mezzanine

As slow control system is being used in the same way as in the CMS tracker and ECAL detectors. A FEC-CCS board in the counting room sends and receives optical control data, on the detector side a Digital Opto-Hybrid Module (DOHM) converts this data back to electrical form and interfaces with the RPMB via two 20pins 3M high speed connectors placed on the front panel. A Communication and Control Unit mezzanine (CCUM) on the RPMB - Figure 6 decodes this information and provides 16 I^2C interface channels and one 8 bit parallel control port for use on the RPMB. All integrated circuits including the VFAT2 are controlled using these I^2C interfaces.

In addition to the slow control information transmitted over I^2C, several sensors mounted on the RPMB or on the hybrids provide additional information like temperature, pressure and radiation dose.

Figure 5 CCUM Mezzanine

4. Control Interface

The control interface on the board is based on CCUM mezzanine and TOTEM Digital Opto-Hybrid Module DOHM. The TOTEM DOHM module is the same as CMS Tracker DOHM with different input/output connectors to RPMB. The CCUM mezzanine provides up to 16 I2C channels. On every channel different number of I2C devices are connected.

4.1. I2C Devices

The following Table 1 shows all devices per I2C channel with their names and addresses:

RPMB I2C Devices			
Channel N:	**Channel Address [HEX] -> Name**	**I2C**	**Device Name**
0	0x10 -> CCUM	0x00	CCU25
1	0x11 -> PLANE1	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU
2	0x12 -> PLANE2	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU
3	0x13 -> PLANE3	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU
4	0x14 -> PLANE4	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU
5	0x15 -> PLANE5	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU
7	0x17 -> PLANE7	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU
8	0x18 -> PLANE8	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU

9	0x19 -> PLANE9	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU
10	0x1A -> PLANE10	0x10	VFAT1
		0x20	VFAT2
		0x30	VFAT3
		0x40	VFAT4
		0x50	DCU
11	0x1B -> DATA	0x00	GOH1
		0x01	
		0x02	GOH2
		0x03	
		0x04	GOH3
		0x05	
		0x06	GOH4
		0x07	
		0x08	GOH5
		0x09	
12	0x1C -> CLOCK/TR_VFAT/CC	0x10	PLL25
		0x20	TR_VFAT
		0x30	CC_ODD
		0x40	CC_EVN
13	0x1D -> SPARE	-	Not Used
14	0x1E -> DOHM	0x70	DOH_A(1) DOH_B(2)
16	0x1F -> SPARE	-	Not Used
(1) DOH-A from first RPMB in the control loop (2) DOH-B from the second RPMB in the			

Table 1 I2C Channels and Devices

The I2C devices are described in details (registers configuration and programming) in the reference documents. Please see the Chapter 10.

In order to provide additional control on the board apart from I2C interfaces the parallel port (PIA) of the CCUM is using.

The configuration of the PIA bits has to be done in such a way that every bit is important for the normal RPMB operation! The modification of single bit requires all the others bits to be well defined according to Tables 2 to 6!

The eight bits has the following assignments, see Table 2:

CCUM Parallel Port Bits			
Bit N:	**Name**	**RPMB Signal**	**Action**
0	BPP1	RES-B	Reset Soft to VFAT's, CC, TR_VFAT
1	BPP2	REH-B	Reset Hard to VFAT's, CC, TR_VFAT
2	BPP3	GOH_FLAG1	Controls GOH's power-up
3	BPP4	GOH_FLAG0	Controls GOH's power-up
4	BPP5	SEL1	Select DVALID from P1 or P9
5	BPP6	SEL2	Select DVALID from P2 or P10
6	BPP7	SEL3	Select DVALID from (P1 or P9) or (P2 or P10)
7	BPP8	SEL4	Select TR_BC0 output

Table 2 CCUM Parallel Port Bits Assignments

It is well known that GOL on the hybrid has start-up problem (see Chapter 11 of the Reference 7). In order to solve this problem special Power Up sequence described on Table 3 has to be applied:

GOH's Power Up Sequence		
N:	**RPMB Signals**	**Action**
1	GOH_FLAG0 and GOH_FLAG1	Write "11" to BPP4 and BPP3 => PIA 0x0C
2	GOH_FLAG0 and GOH_FLAG1	Write "10" to BPP4 and BPP3 => PIA 0x08
3	RESETOUTZ	Generate CCUM RESETOUTZ output via CRA register

Table 3 Control of GOH's Power Up sequence

In the Chapter 11 of "GOL Reference Manual" is written: ***"... It is very important to minimize the transition time between the on/off states. The CRT4T transistors are capable of handling rather high currents. If the transition time between the two states is long a large current will flow through the power supply casing potential damage to the circuit or the system where it is inserted."*** That is why the time for execution the sequences 1 to 3 from Table 3 is mandatory to be kept as short as possible. This can be done with three commands from the FEC to the corresponding RPMB; therefore the commands have to be consecutive.

The Trigger VFAT BC0 output enable sequence is described on Table 4:

Trigger VFAT BC0 output enable		
N:	**RPMB Signals**	**Action**
1	SEL4	Write "0" to BPP8
2	-	Configure the Trigger VFAT chip for BC0 output

Table 4 Trigger VFAT BC0 output enable

General reset (hard or soft, see Ref. 2) can be applied to all VFATs on the planes. The sequence for doing that is described on Table 5:

VFAT resets (hard and soft)		
N:	**RPMB Signals**	**Action**
1	RES-B	Write "0" to BPP1 (soft reset)
2	REH-B	Write "0" to BPP2 (hard reset)

Table 5 VFAT resets

There are possibilities to select Data Valid (DVALID) signals from four different plates. After selection the signal is used as global data GOHs enable for the transmissions. The DVALID selection is described on Table 6. After power ON and CCUM initialization the default DVALID is selected from Plane 10.

VFAT Data Valid (DVALID) selection		
N:	**RPMB Signals**	**Action**
1	SEL3, SEL2, SEL1	Write “0X0” to BPP7, BPP6, BPP5 to select DVALID from P1
2	SEL3, SEL2, SEL1	Write “0X1” to BPP7, BPP6, BPP5 to select DVALID from P9
3	SEL3, SEL2, SEL1	Write “10X” to BPP7, BPP6, BPP5 to select DVALID from P2
4	SEL3, SEL2, SEL1	Write “11X” to BPP7, BPP6, BPP5 to select DVALID from P10

Table 6 VFAT Data Valid (DVALID) selection

5. Data Output Interface

5.1. Block Structure

The data output interface is built using the data conversion and transmission blocks. Four serial data outputs from every plane in LVDS signal levels format are being converted to CMOS level using CRT910 chips. Then, 40 data bits are entering three GOH’s 16bit each, to be serialized and sent to the counting room. For synchronization of the data stream programmable data valid (DVALID) signal from the VFAT’s is being used to enable the GOH hybrids.

5.2. Data Format

The data format is defined by the VFAT2 and it is presented on Figure 7.

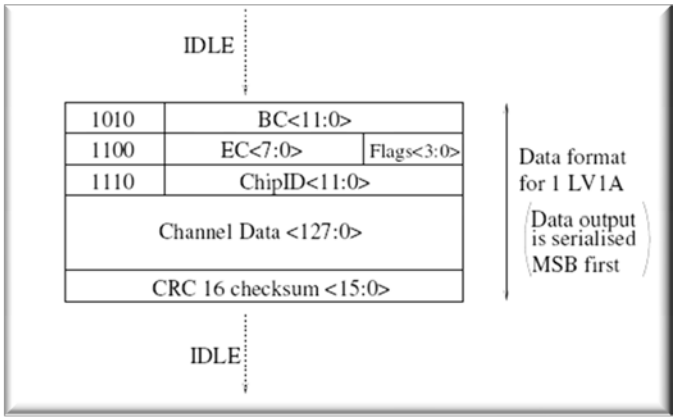

Figure 6 VFAT data format for one trigger

The data sent by the VFAT2 front end chips upon a level 1 trigger signal is converted from LVDS to CMOS on the RPMB and then presented to the gigabit optical hybrids GOH modules, which serialize and convert the electrical data to optical for transmission to the Data Acquisition (DAQ)

system in the counting room. Three GOH mezzanines – Figure 7 are used to send data from 40 VFAT2 chips.

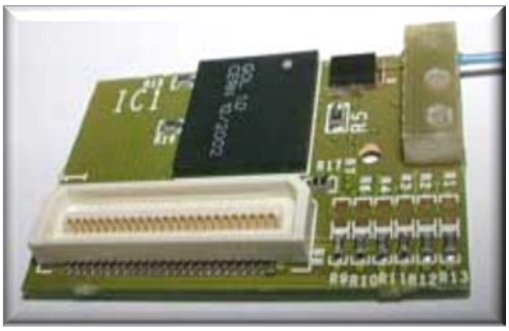

Figure 7 GOH Mezzanine

6. Trigger Output Interface

6.1. Block Structure

The zoom on trigger outputs scheme from RPMB block diagram is on Figure 7.

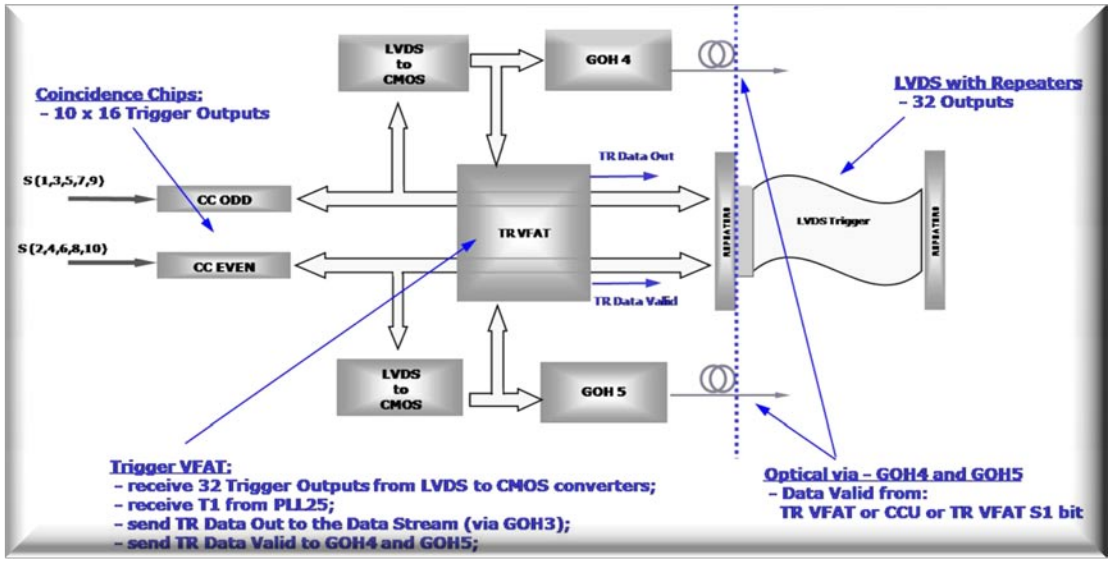

Figure 8 Zoom on Trigger Outputs

6.2. Trigger Bits

Each VFAT2 front end chip has 8 trigger outputs, 4 of which are used in the Roman Pots. Every hybrid therefore generates 16 trigger outputs, and 5 hybrids have the same orientation of the silicon strips (U coordinate), and the 5 others have strips oriented at 90 degrees (V coordinate). The trigger signals are put into coincidence in two separate Coincidence Chips (see Reference 4) , one for the U and one for the V coordinate. The CC chips are mounted on the RPMB as mezzanine cards (CC mezzanine), one mezzanine per CC. The CC provides 16 outputs (so the number of trigger signals is reduced from 2x80 to 2x16), and these signals have to be transmitted to the counting room.

The latency constraints on the generation of the trigger bits especially from the Roman Pots are very severe: after subtraction of cable delays only about 8-10 bunch crossings are left for the generation of the trigger signals to be provided to CMS from the signals generated by the Roman Pot. A full custom chip with dedicated logic can implement the required coincidence in one clock.

Two GOH mezzanines send the trigger bits optically to the counting room. They are used in the optical trigger system.

7. Environmental Interfaces

7.1. RADMON Carrier

The RADMON carrier is made of a thin (~500 m) double-sided PCB. It can host up to 5 *p-i-n* diodes and can allow the readout of five RadFETs mounted inside a proper package. A total of 11 devices, including a temperature sensor (10k NTC), can be mounted on the integrated sensor PCB and readout via a 12-way flat cable: 11 for sensor signals and a common Return Line (RL) connection.

The on-board connector is an ERNI Male SMC-B 12 contacts (model 054594). The overall dimensions of the assembled PCB, including the connector plug, are of about 34 mm × 15 mm × 4 mm. See more details in [8].

Figure 9 RADMON Carrier

7.2. Temperature and Pressure Sensors

PT100/1000 sensors are used for temperature, and a piezoelectric pressure sensor measures the pressure inside the pot to verify the pressure remains close 0 (a secondary vacuum has to be maintained in the Roman Pot).

8. Power

The RPMB needs to receive low voltage power at 2.5 V for its own operation, and for the operation of the hybrids. The power on the hybrids has been carefully separated between analogue and digital blocks, both powered at 2.5 V. Two LV channels per RPMB are foreseen, one for digital DVDD and another for analogue AVDD power, which is distributed on the board and also on the RP Hybrids. On the motherboard the two grounds DGND and AGND are connected together.

In order to provide power to the control circuitry CCUM, third LV channel is provided from Digital OptoHybrid Module – DOHM via the control loop cables. This allows to power only the control part of the board and check the control loop functionalities.

The silicon detectors need to be biased up to 500 V after irradiation. The RPMB receive this high voltage supply and distributes it to the detector hybrids. The supply is separate for all detectors; grouping is done in the counting room.

9. References

1. CCU25 - Communication and Control Unit
2. VFAT - VFAT2 - Logical functionality (Version 9) (also for TR_VFAT)
3. DCU - DCU2 User Guide
4. CC - Coincidence Chip Specification (for CC_ODD, CC_EVN)
5. PLL25 - CMS Tracker PLL Reference Manual
6. DOH - Front-end Digital Opto-Hybrid
7. GOH - GOL Reference Manual
8. RADMON - TOTEM on-line Radiation Monitoring System